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High-Speed  
Memory Systems

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Spring 2014

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CS-590.26  
Lecture F

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Bruce Jacob

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University of Crete

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SLIDE 1

**CS-590.26, Spring 2014**

***High-Speed Memory Systems:  
Architecture and Performance Analysis***

**ONFI 3.2 and  
Flash Control Basics**



# Open NAND Flash Interface—Basics

**The command set**

**Addressing and activation**

**Figuring out what you're attached to**

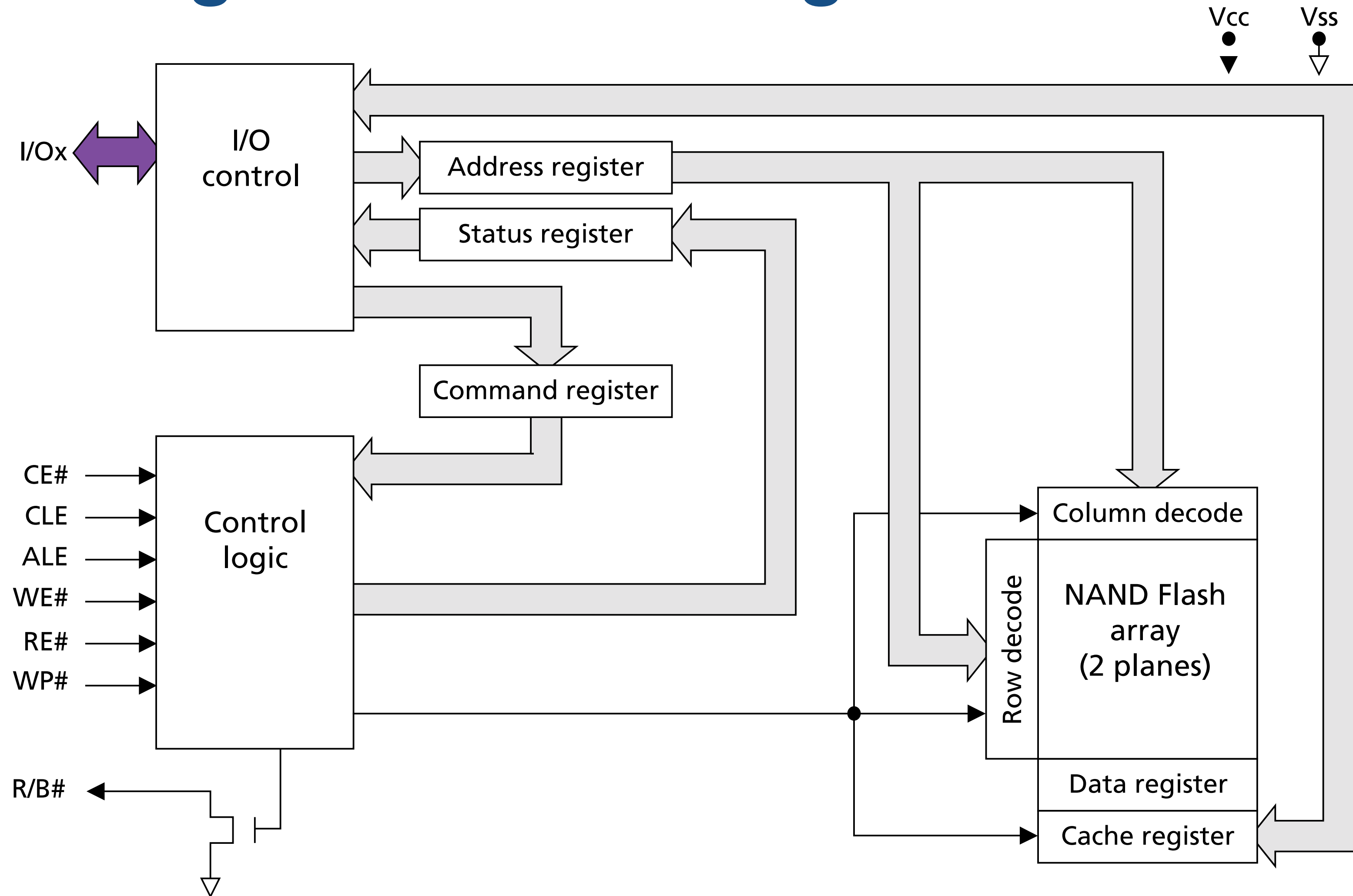
**Command overview, including concurrent accesses**

**NV-DDR and NV-DDR2 interfaces**



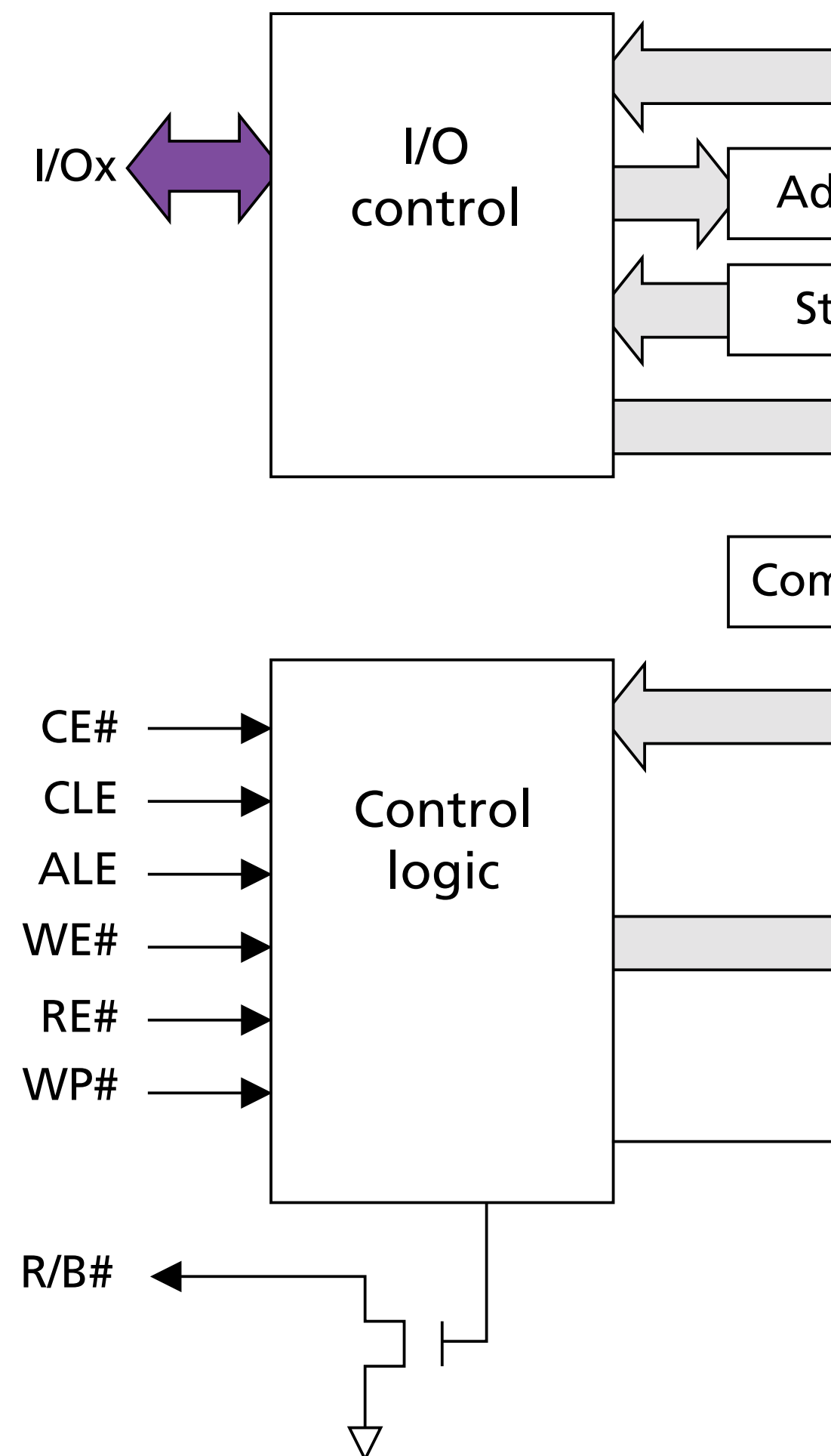


# Recall general device organization





## Recall general device organization



**Control signals ('#' = *active low*)**

**CE#** – Chip Enable

**CLE** – Command Latch Enable

**ALE** – Address Latch Enable

**WE#** – Write Enable

**RE#** – Read Enable

**WP#** – Write Protect

**R/B#** – Read/Busy (from SR[6])

**There is also a CLK ...**



## Three Interfaces:

### SDR

- what used to be called “asynchronous”
- can be 8-bit or 16-bit
- relatively slow

### NV-DDR

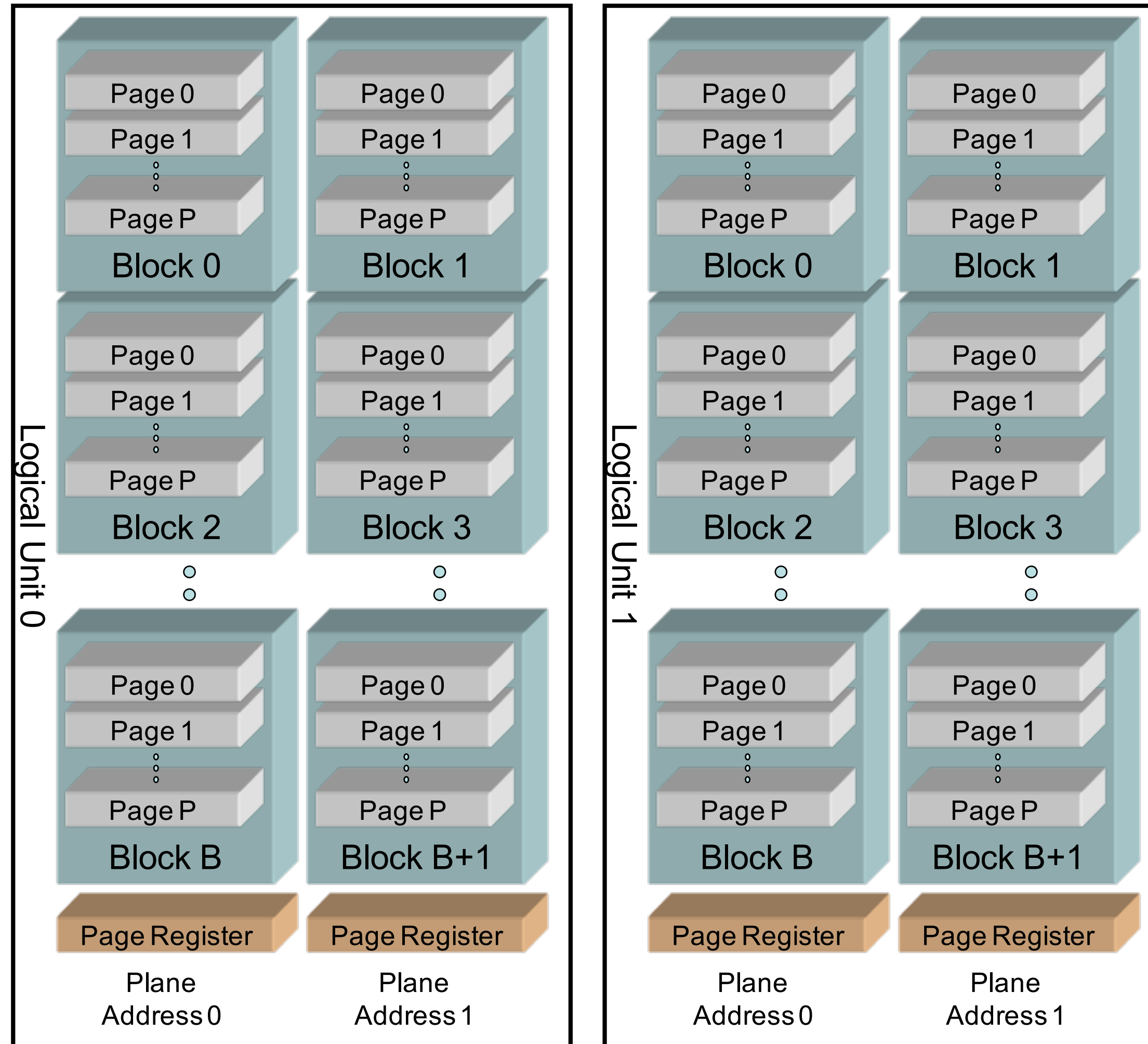
- used to be called “source-synchronous”
- must be 8-bit
- up to 100MHz, 200MT/s = 200MB/s

### NV-DDR2

- must be 8-bit
- up to 267MHz, 533MT/s = 533MB/s



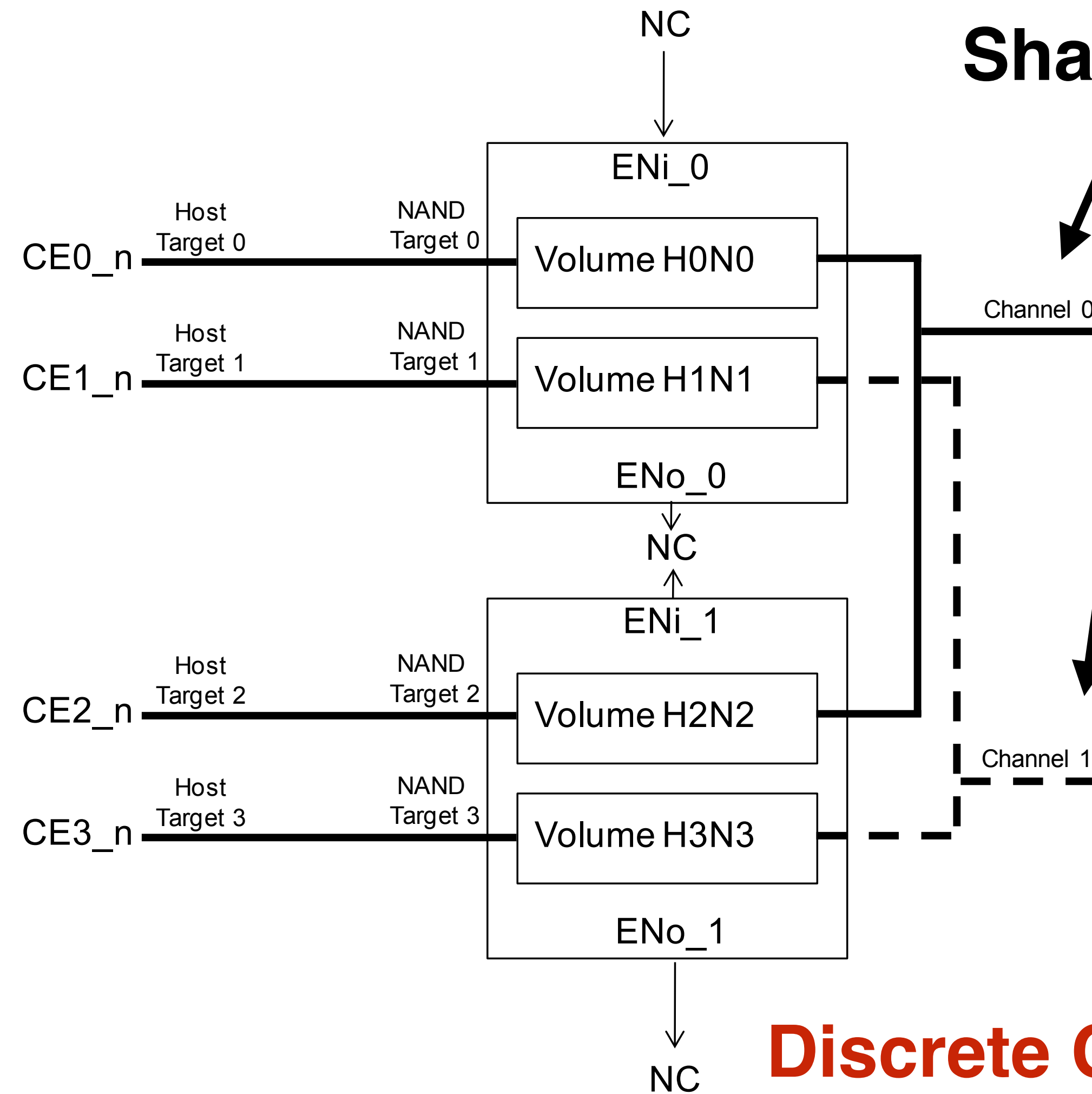
# 1 pkg: 1–32 dies, 1–4 I/O buses, 1–32 CEs



**“Page Register”**



# Several ways to group internal devices I



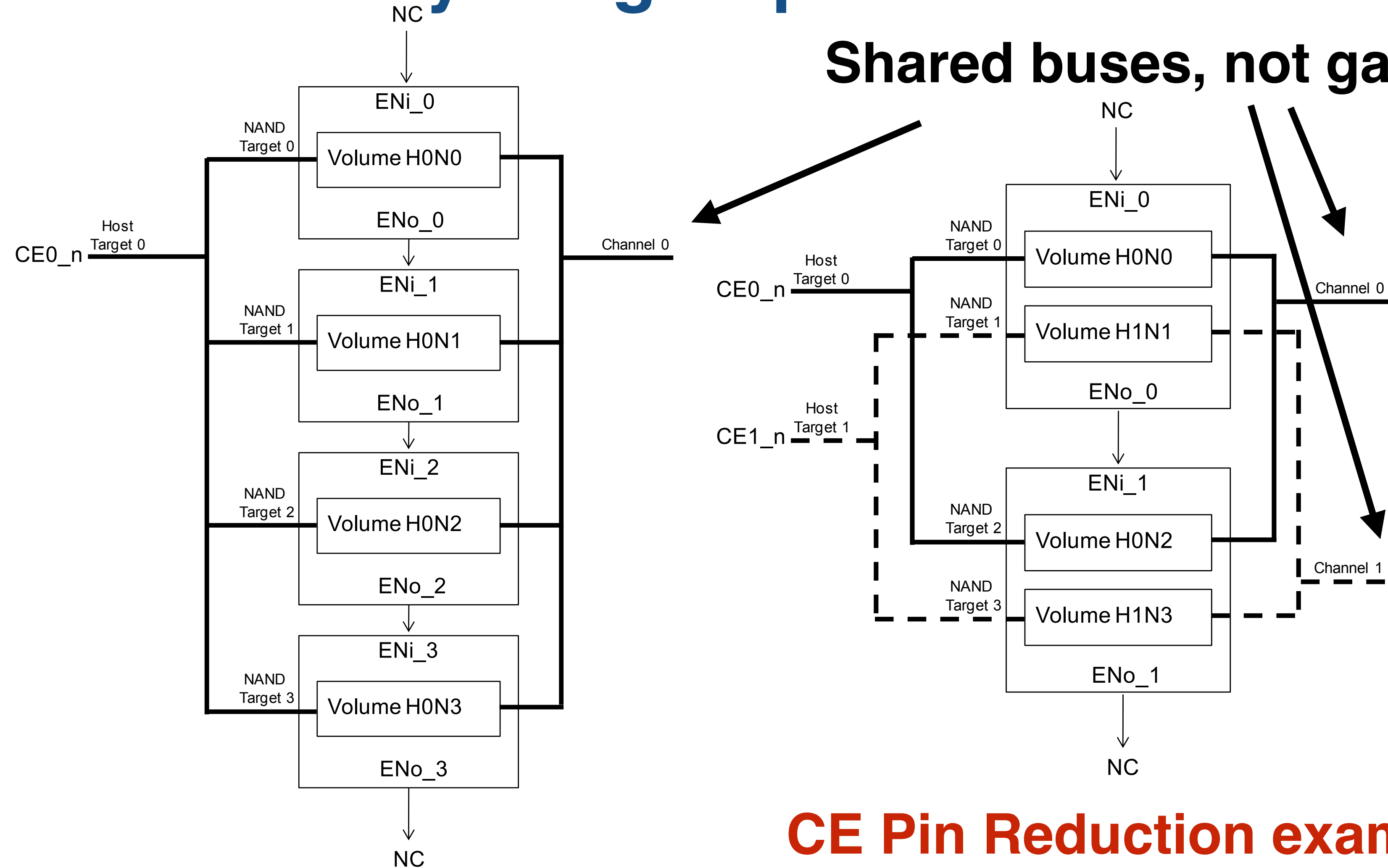
**Shared buses, not ganged**

**Discrete CE per device example**



# Several ways to group internal devices II

## Shared buses, not ganged

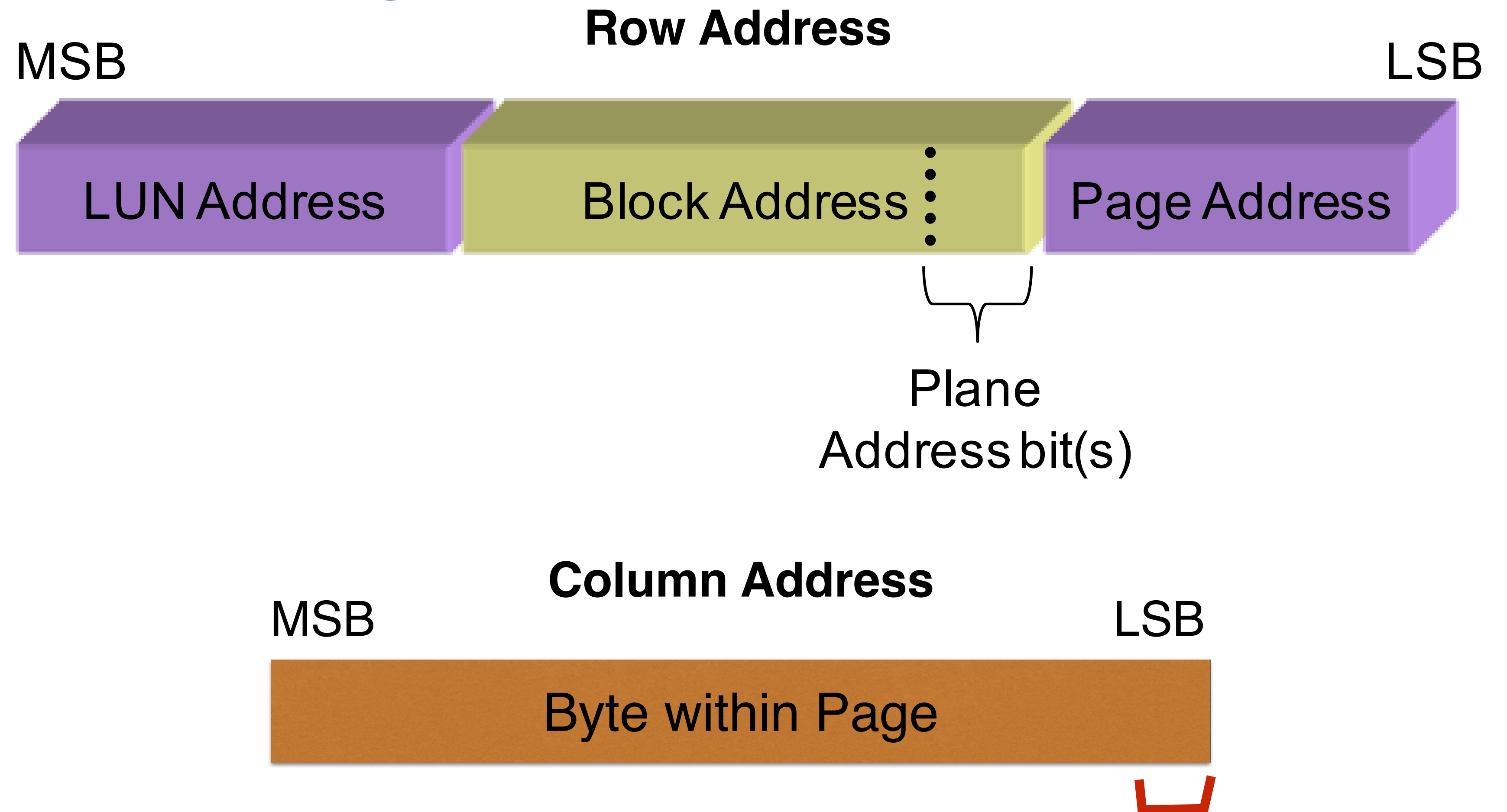


**CE Pin Reduction examples**





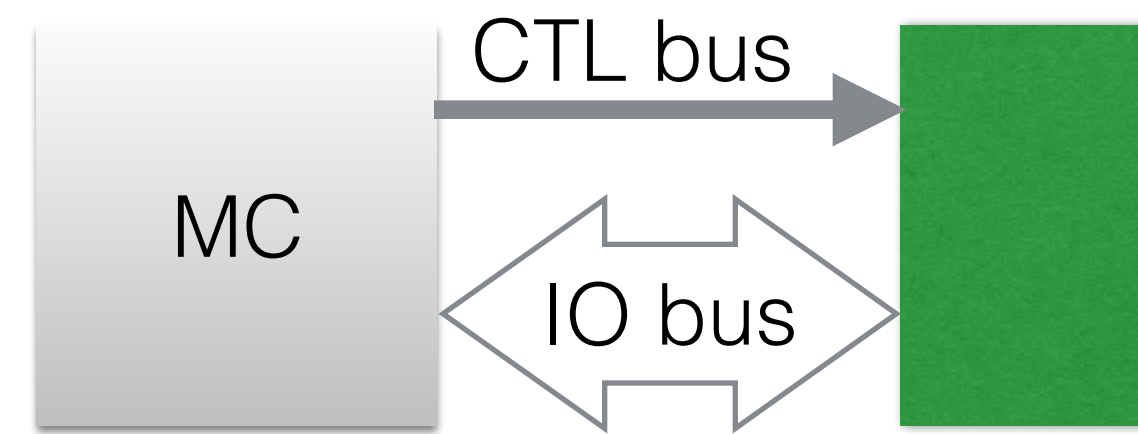
# Addressing



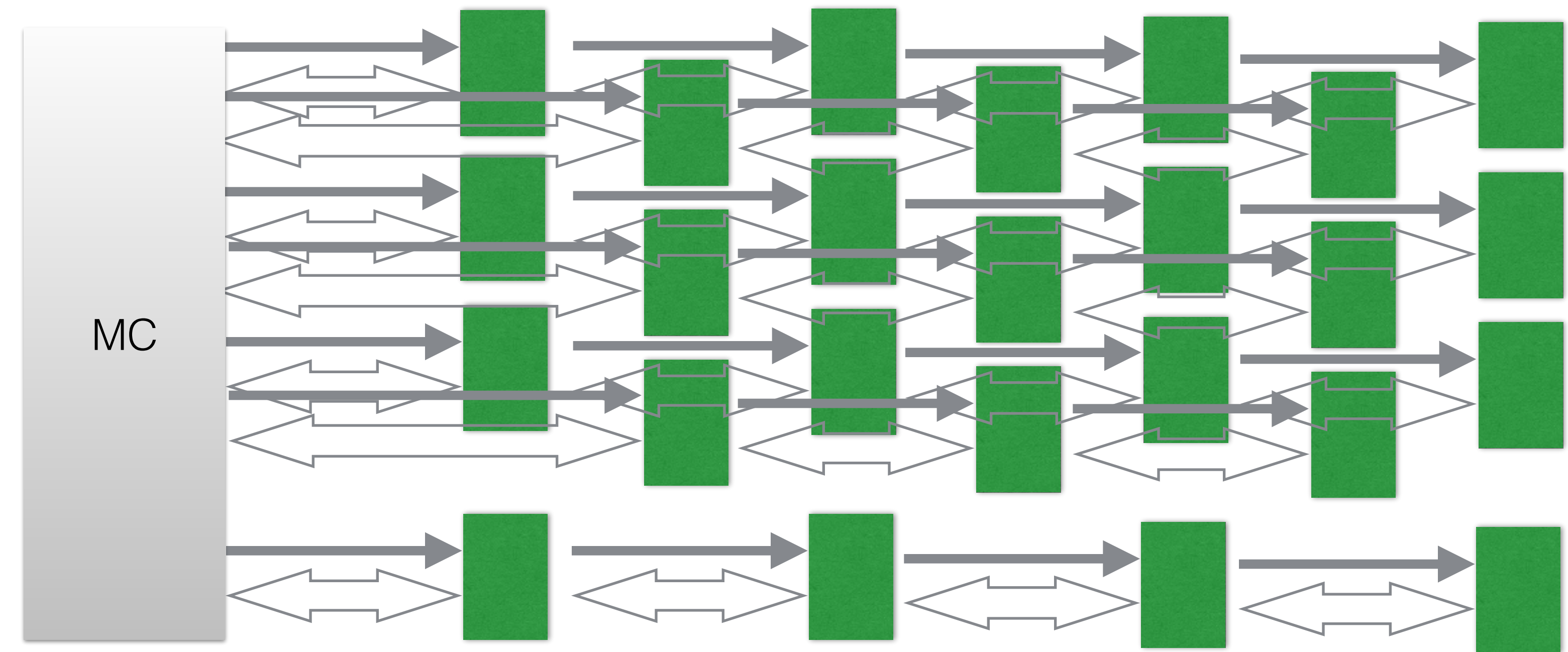
**Note: Least significant column bit must be 0 for DDR interfaces**



## This is easy

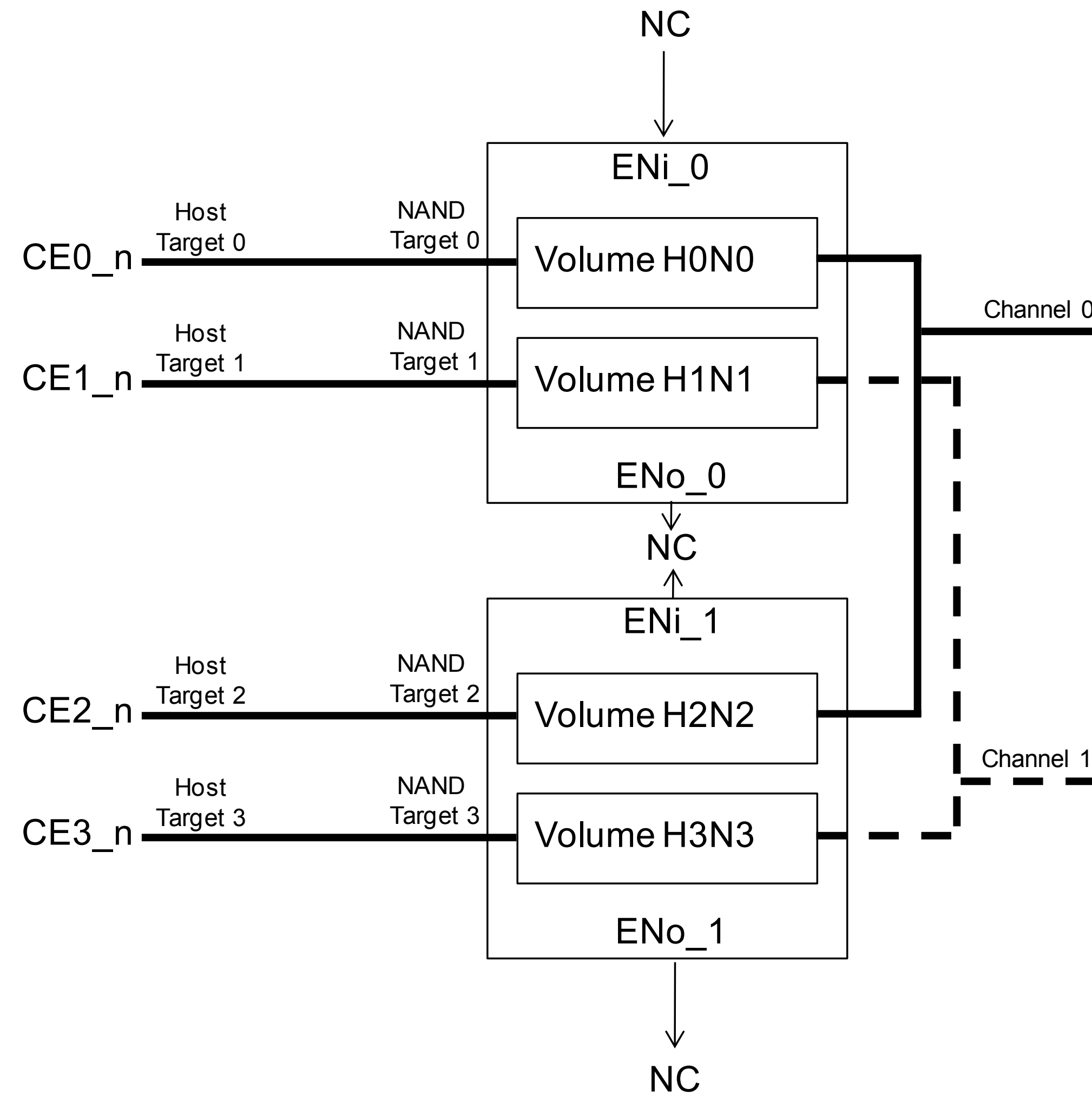


## This is not





# Config I: Discrete CE per Device





## Config I: Discovery

**Foreach distinct CE pin  $i$ , in order from CE\_0 to CE\_7:**

**Foreach distinct 8-bit bus  $j$  (could be up to 4):**

**Pull CE\_ $i$  low**

***Using I/O Bus  $j$ :***

**Issue Reset (FFh) command**

**Issue Read ID (90h) command with address 20h**

**If ONFI signature is returned**

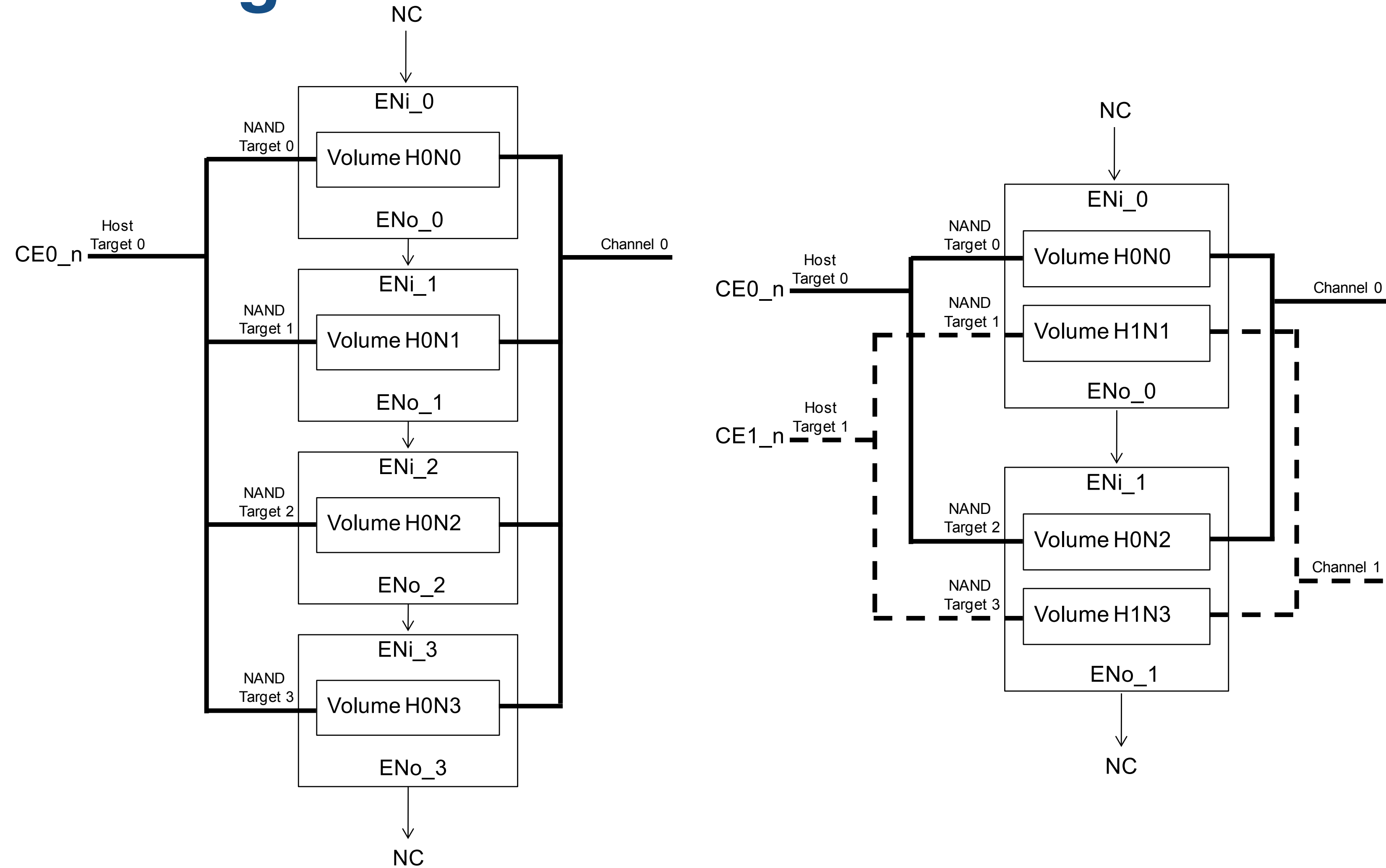
**Make a note that **CE\_ $i$  + Bus  $j$**  is valid combo**

**Next CE pin**

**else ...**



# Config II: CE Pin Reduction



## Config II: Discovery

1. Power is applied to the NAND device(s).
2. CE<sub>n</sub> (Host Target) is pulled low.
3. If resetting all NAND Targets in parallel, then the host issues the Reset (FFh) command. This command is accepted by all NAND Targets connected to the CE<sub>n</sub> (Host Target).
4. If resetting each NAND Target sequentially, then:
  - a. Host issues Read Status (70h) command. Issuing Read Status (70h) prior to any other command indicates sequential Reset (FFh) of each NAND Target.
  - b. Host issues Reset (FFh). This command only resets the NAND Target connected to the CE<sub>n</sub> (Host Target) whose EN<sub>i</sub> signal is high.
5. Host issues Read Status (70h) command and waits until SR[6] is set to one.
6. Host configures the NAND Target. Read ID, Read Parameter Page, and other commands are issued as needed to configure the NAND Target.
7. Set Feature with a Feature Address of Volume Configuration is issued to appoint the Volume address for the NAND Target(s) whose EN<sub>i</sub> signal is high. The Volume address specified shall be unique amongst all NAND Targets. After the Set Features command completes, EN<sub>o</sub> is pulled high and the Volume is deselected until a Volume Select command is issued that selects the Volume. The host shall not issue another command to a NAND Target connected to the associated Host Target until after tFEAT time has elapsed.
8. For each NAND Target connected to the Host Target, steps 4-7 are repeated for the sequential initialization sequence and steps 5-7 for the parallel initialization sequence.
9. When no further NAND Targets are found connected to the Host Target, then repeat steps 2-8 for the next Host Target (i.e. host CE<sub>n</sub> signal).
10. To complete the initialization process, a Volume Select command is issued following a CE<sub>n</sub> transition from high to low to select the next Volume that is going to execute a command.



## Config II: Discovery

### Basic idea:

**Go through and assign a different Volume Address (via Set Features) to each device on the same CE line**

**Thereafter, each time you want to execute a given command (Read, Program, Erase, etc.) you need to pull CE low and execute a Volume Select command first**





# ONFI Cmd Set

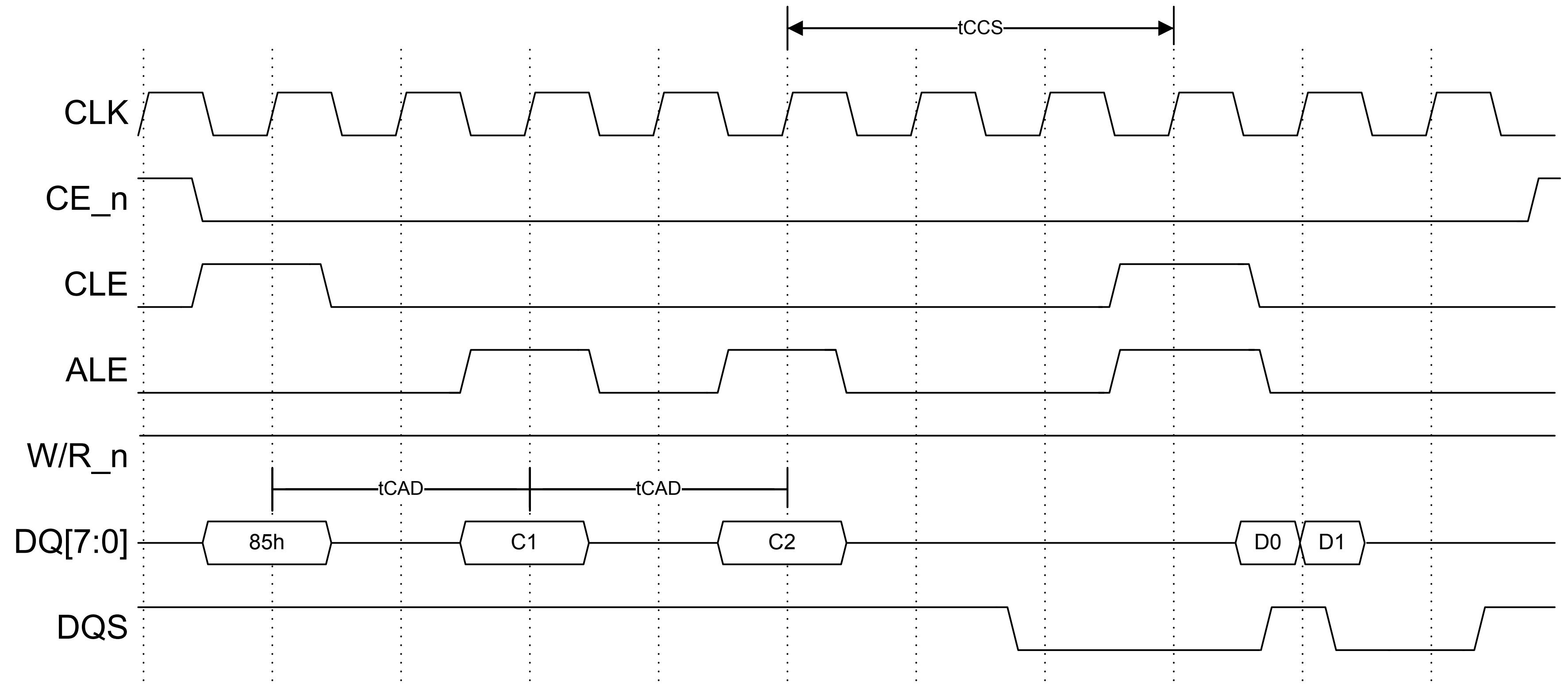
- Read**
- Change Read Column**
- Read Cache**
- Page Program**
- Page Cache Program**
- Block Erase**
- Read Status**
- Read ID**
- Read Parameter Page**

Command	O/M	1 <sup>st</sup> Cycle	2 <sup>nd</sup> Cycle	Acceptable while Accessed LUN is Busy	Acceptable while Other LUNs are Busy	Target level commands
Read	M	00h	30h		Y	
Multi-plane	O	00h	32h		Y	
Copyback Read	O	00h	35h		Y	
Change Read Column	M	05h	E0h		Y	
Change Read Column Enhanced	O	06h	E0h		Y	
Read Cache Random	O	00h	31h		Y	
Read Cache Sequential	O	31h			Y	
Read Cache End	O	3Fh			Y	
Block Erase	M	60h	D0h		Y	
Multi-plane	O	60h	D1h		Y	
Read Status	M	70h		Y	Y	
Read Status Enhanced	O	78h		Y	Y	
Page Program	M	80h	10h		Y	
Multi-plane	O	80h	11h		Y	
Page Cache Program	O	80h	15h		Y	
Copyback Program	O	85h	10h		Y	
Multi-plane	O	85h	11h		Y	
Small Data Move <sup>2</sup>	O	85h	11h		Y	
Change Write Column <sup>1</sup>	M	85h			Y	
Change Row Address <sup>1</sup>	O	85h			Y	
Read ID	M	90h				Y
Volume Select <sup>3</sup>	O	E1h		Y	Y	
ODT Configure <sup>3</sup>	O	E2h				Y
Read Parameter Page	M	ECh				Y
Read Unique ID	O	EDh				Y
Get Features	O	EEh				Y
Set Features	O	EFh				Y
LUN Get Features	O	D4h			Y	
LUN Set Features	O	D5h			Y	
Reset LUN	O	FAh		Y	Y	
Synchronous Reset	O	FCh		Y	Y	Y
Reset	M	FFh		Y	Y	Y



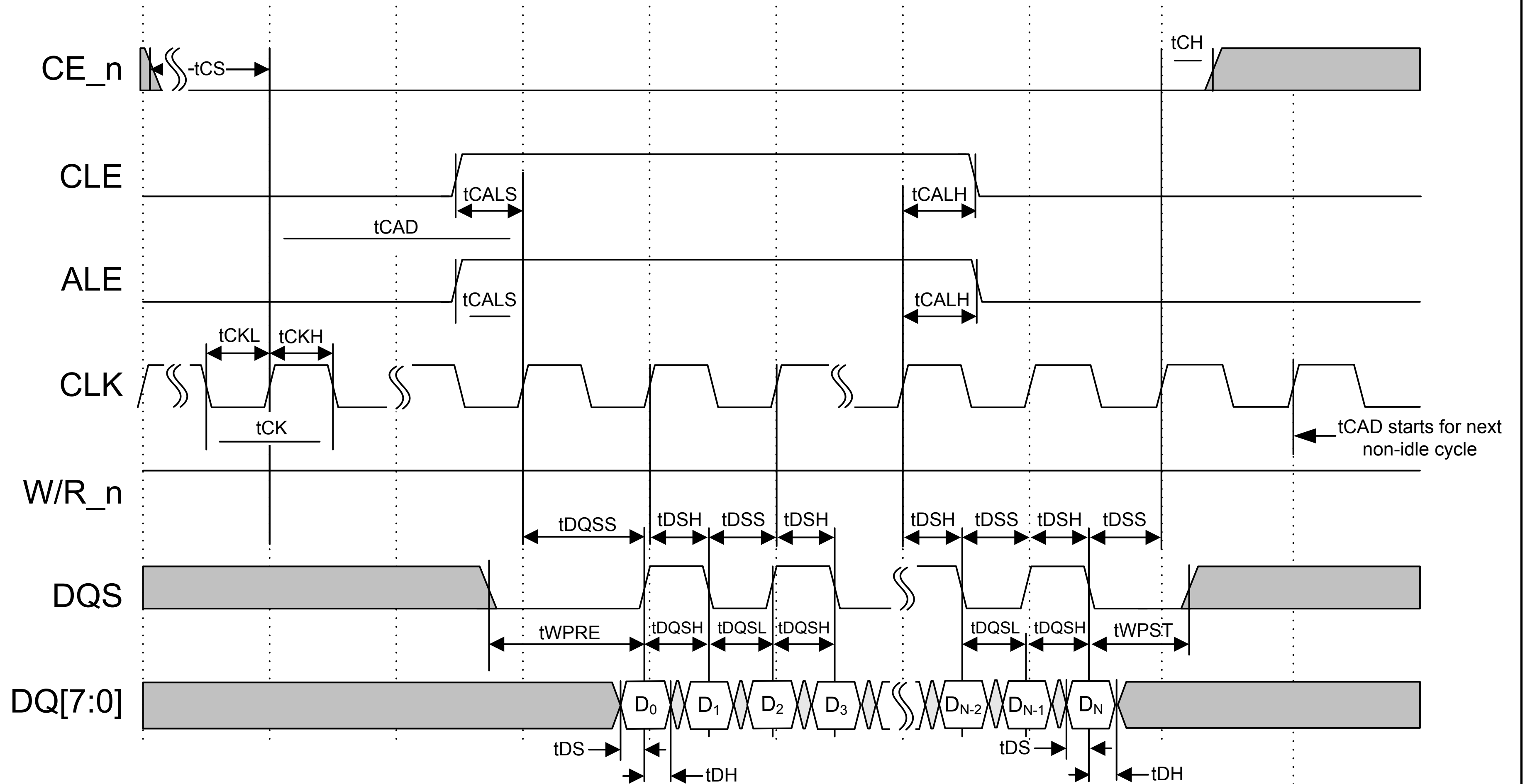


# Sending a Command (NV-DDR)

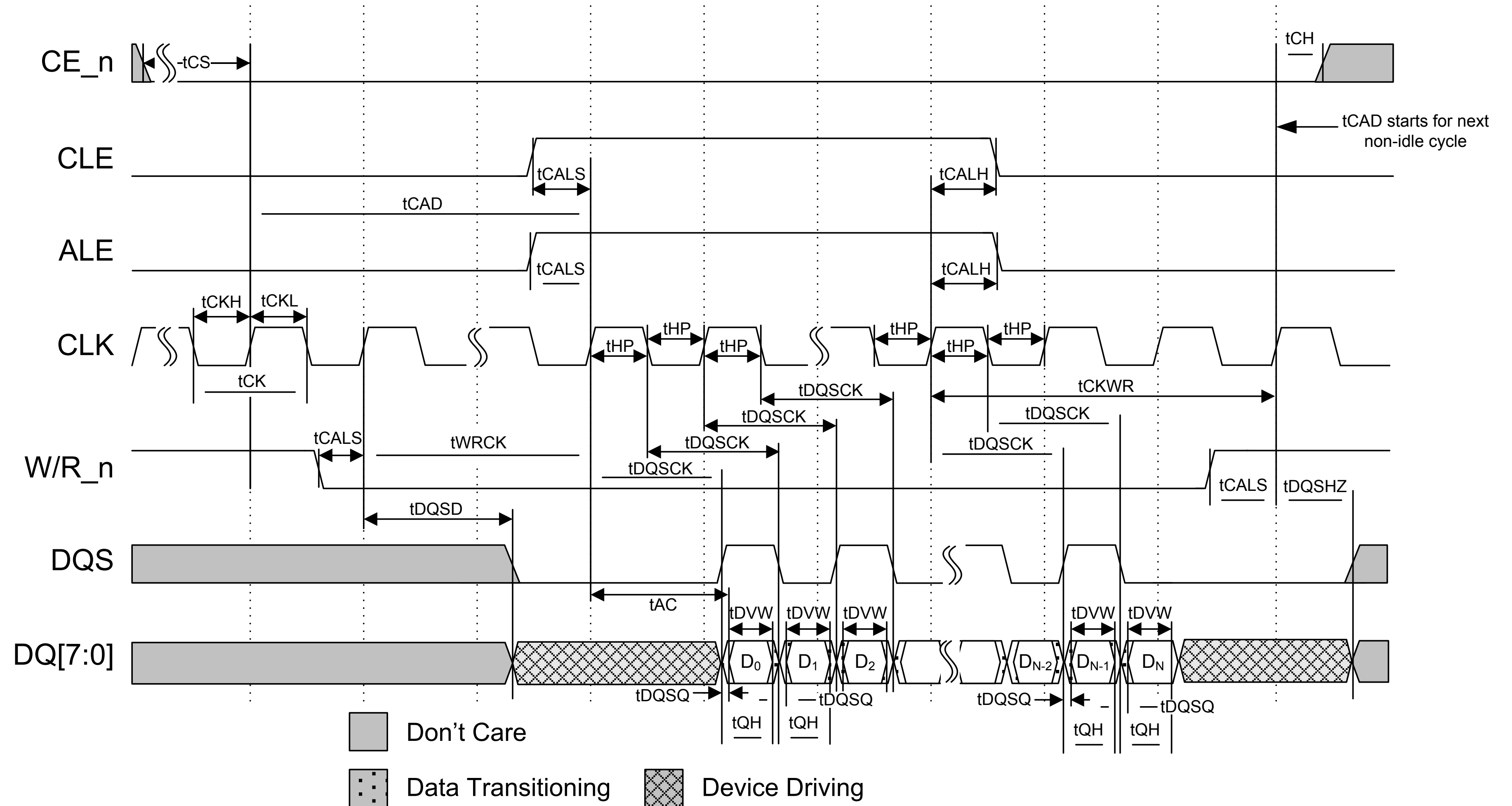




# Data Input to Flash Device

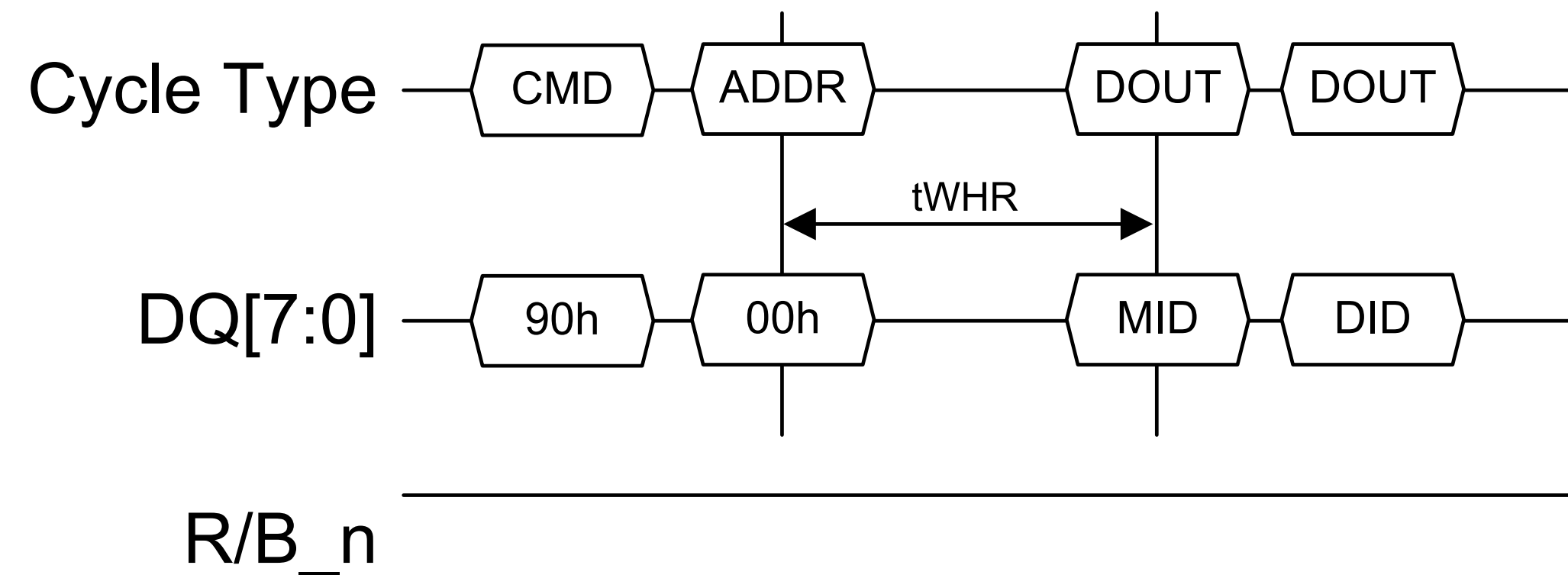


# Data Output from Flash Device

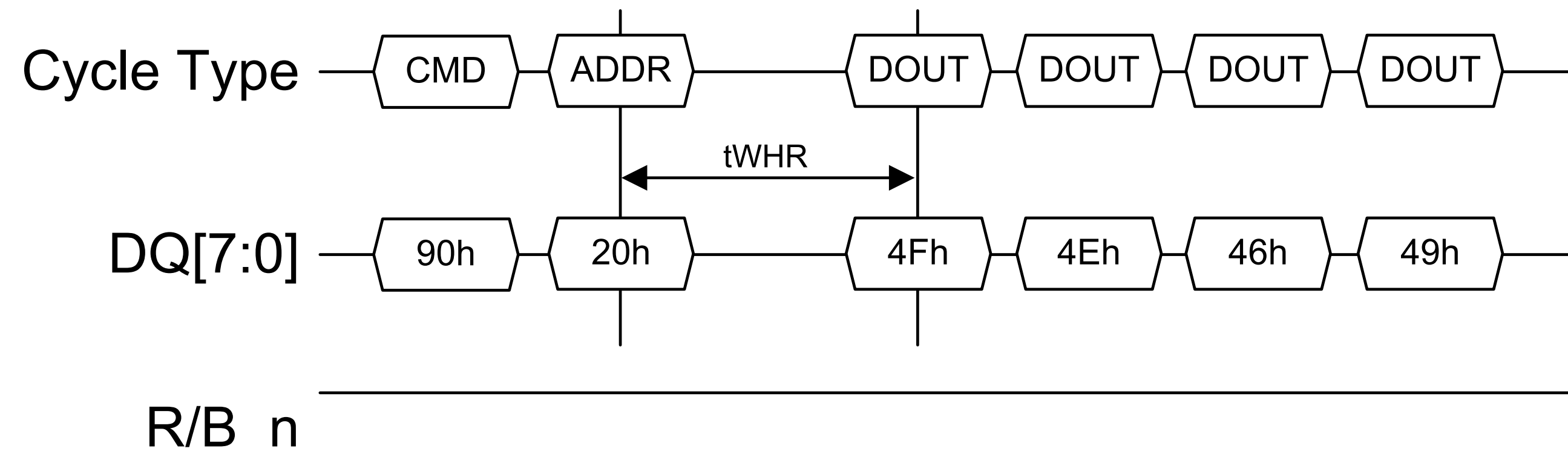


# Read ID

## Address 00h — Manufacturer & Device IDs (2 bytes)



## Address 20h — 'O' 'N' 'F' 'I' (4 bytes)



## Read Parameter Page

**Like Read ID, but returns 256-byte Parameter Page +more**

**Revision number, features supported**

**Manufacturer, product codes**

**Data bytes per page, spare bytes per page**

**Pages per block, blocks per LUN, number of LUNs**

**Number of address cycles: row and column**

**Number of bits per cell, number of planes**

**Endurance info, bad block info, ECC info**

**SDR, DDR, DDR2 timing mode support**

**Electrical parameters, timing parameters, driver strength**

**CRC bits at end**

**... plus, redundant copies of everything**





## Read Status

**Returns the status of the last command processed**

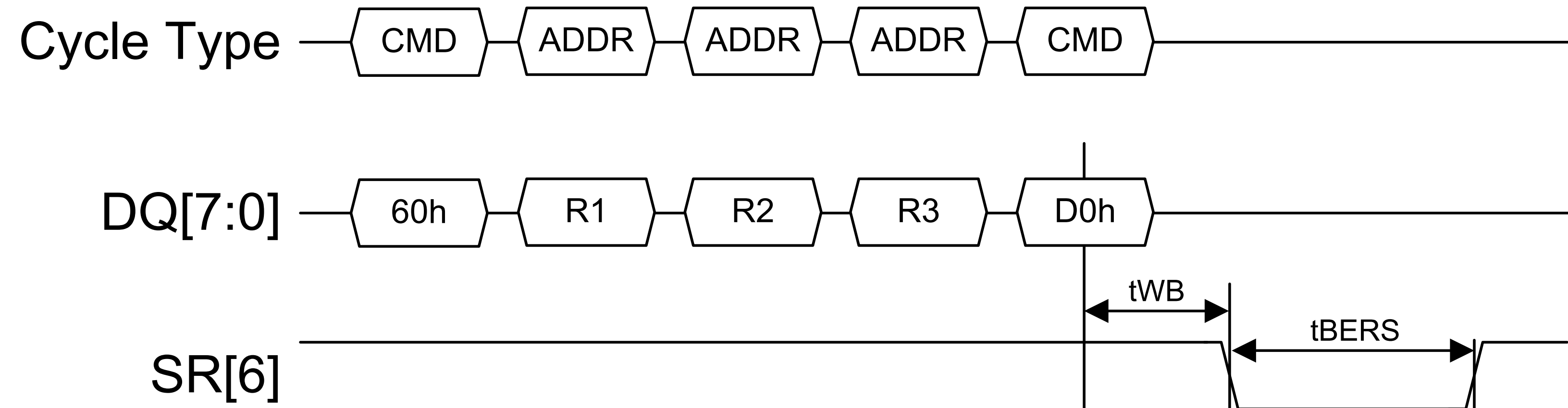
Value	7	6	5	4	3	2	1	0
Status Register	WP_n	RDY	ARDY	VSP	CSP	R	FAILC	FAIL

FAIL last command failed  
FAILC previous command failed  
R reserved  
CSP command-specific  
VSP vendor-specific  
ARDY Array Ready (if 1, no array operation in progress)  
RDY if 1, LUN is ready for a command  
WP\_n write-protect (active low)

**“Enhanced” version specifies row address**

## Block Erase

**R1...R3 is row address (identifies device, block, page)**



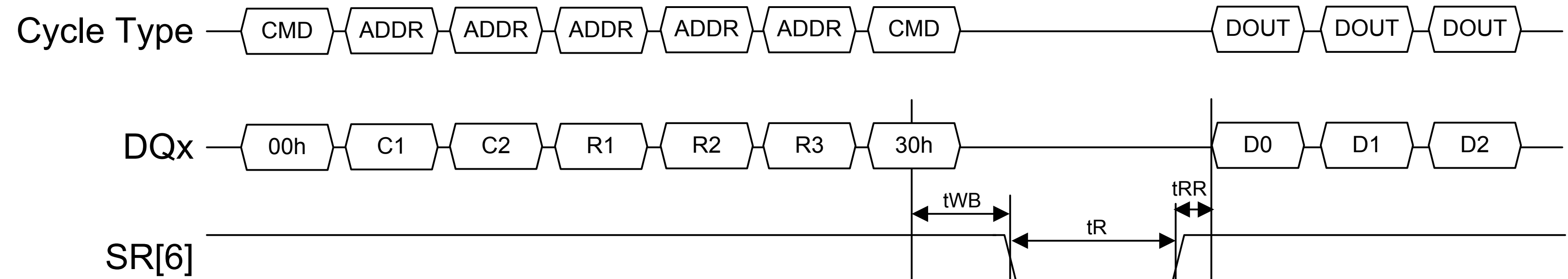
**Successful if SR[0] (FAIL) is zero afterward**

**Host may not attempt to erase a bad block  
(i.e., it is the responsibility of the controller  
to know bad-block information & keep it up to date)**



# Read Page

**C1...C3 is column address; R1...R3 is row address**



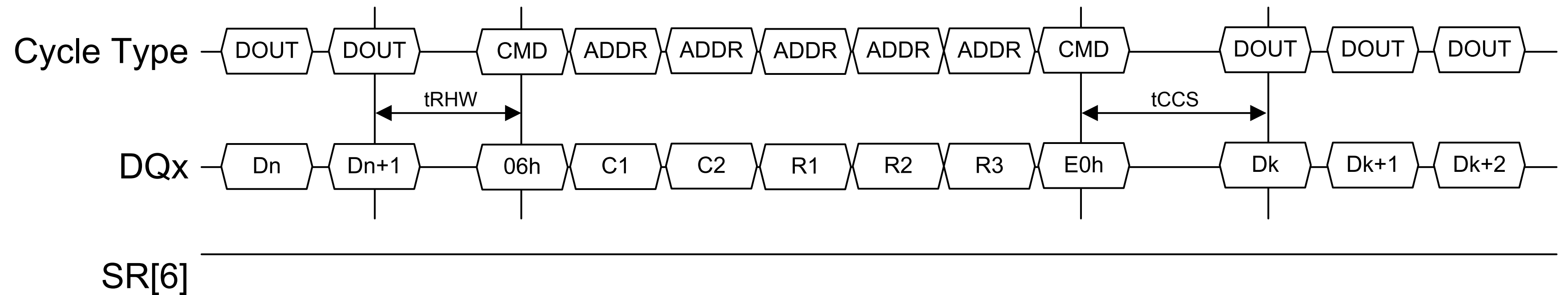
**After  $t_R$  (array-to-register), data is valid to be read out; controller should check the validity before bus transfer (via Read Status Enhanced)**

**Second issuance of 00h starts data read-out on IO bus**





## Change Read Column (Enhanced)



**USE:** **Read Page** command issued to LUN 0

**Read Page** command issued to LUN 1

**Read Status Enhanced** selects LUN 0

**Change Read Column (Enhanced)** issued to LUN 0

Data transferred from LUN 0

**Read Status Enhanced** selects LUN 1

**Change Read Column (Enhanced)** issued to LUN 1

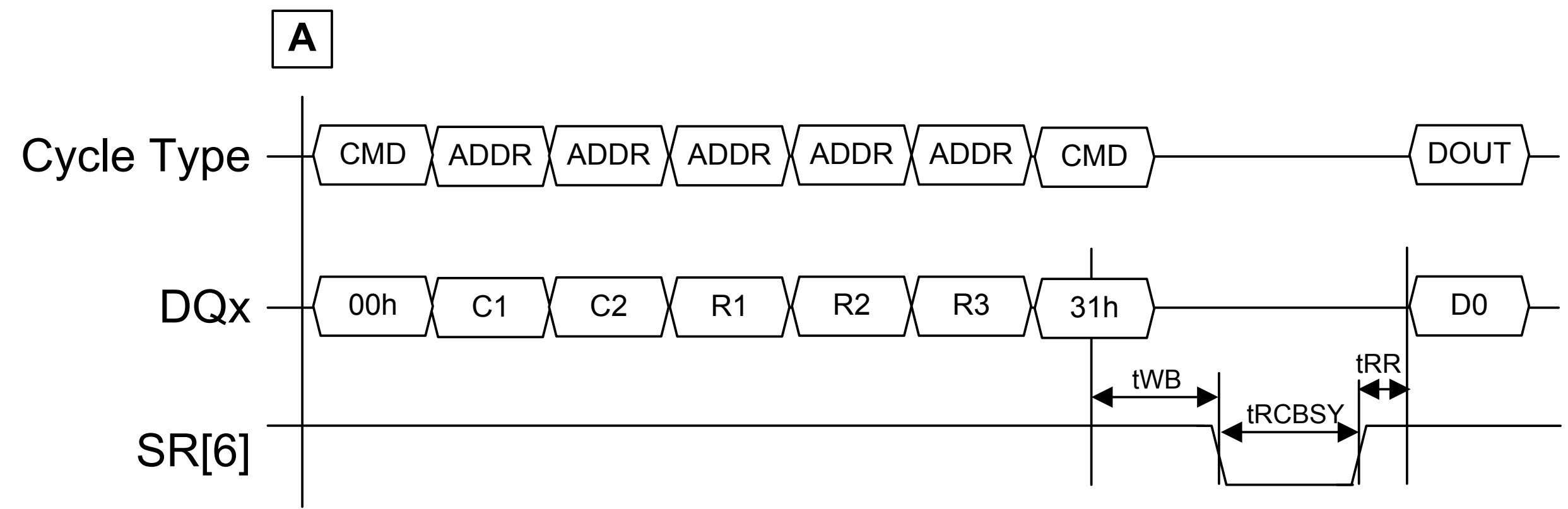
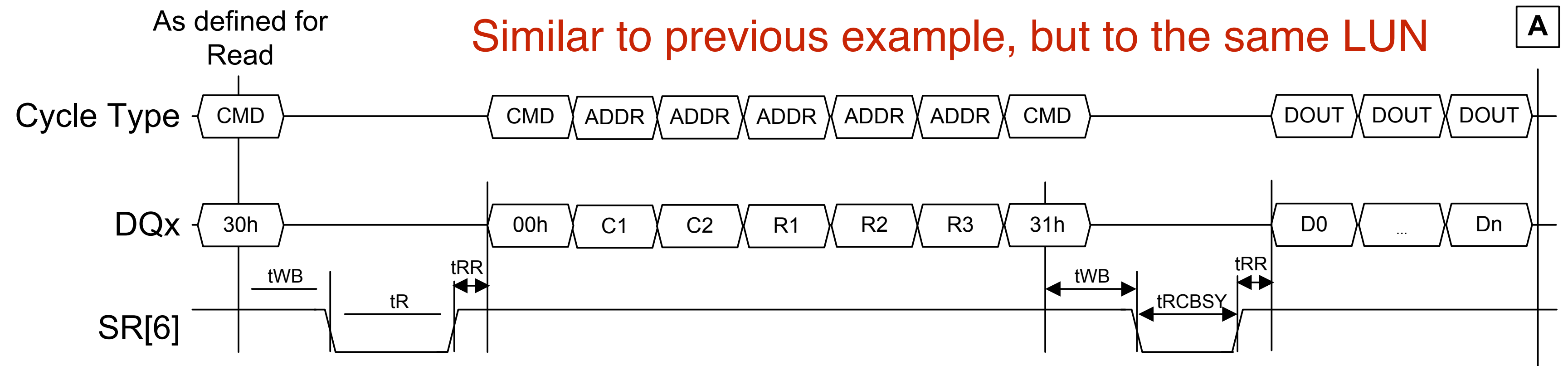
Data transferred from LUN 1



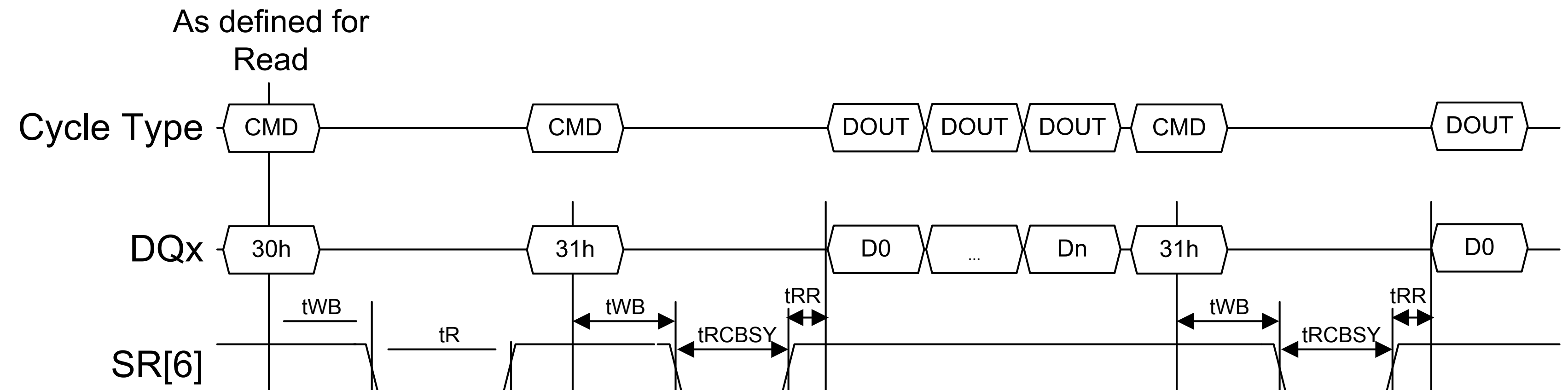


# Read Cache (Random, Sequential, End)

## Read Cache Random (31h):

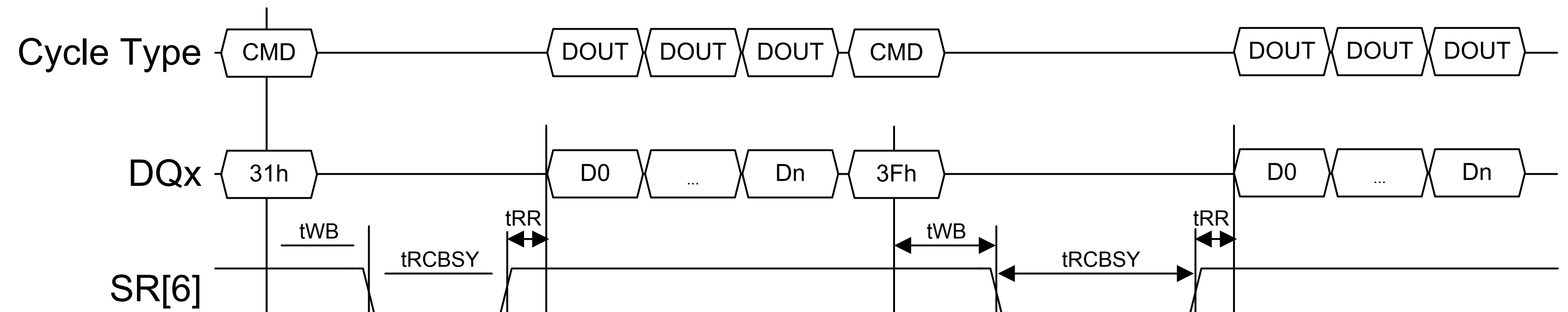


## Read Cache Sequential (31h without address):

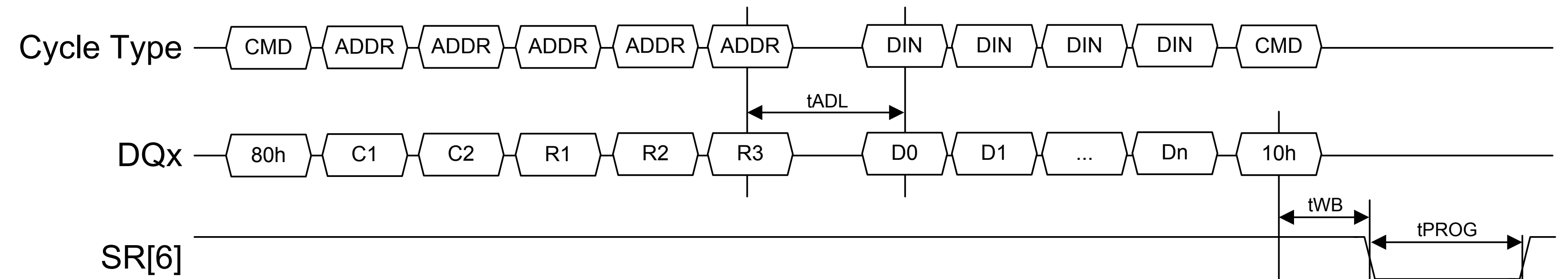


## Read Cache End (3Fh):

As defined for  
Read Cache  
(Sequential or Random)



# Page Program



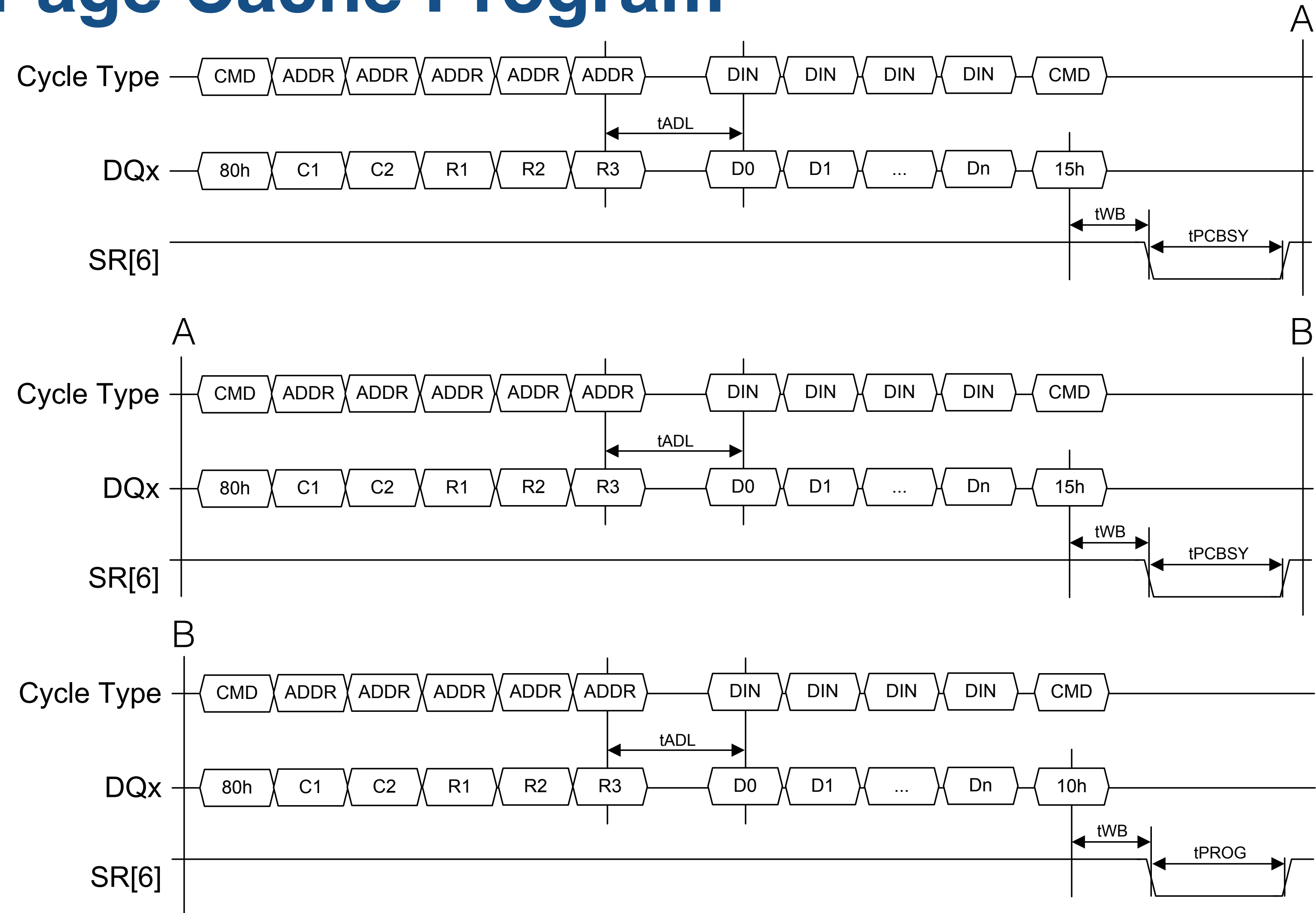
**For operating one plane at a time**

**For operating two or more planes ...  
(to overlap multiple program operations in time)**





# Page Cache Program



## Other interesting commands

**Copyback** (page copy within a single device)

**Small Data Move** (write less than a full page)

**Volume Select** (for addressing many devices on a CE)

**Get/Set Features** (to read/change a device's parameters)

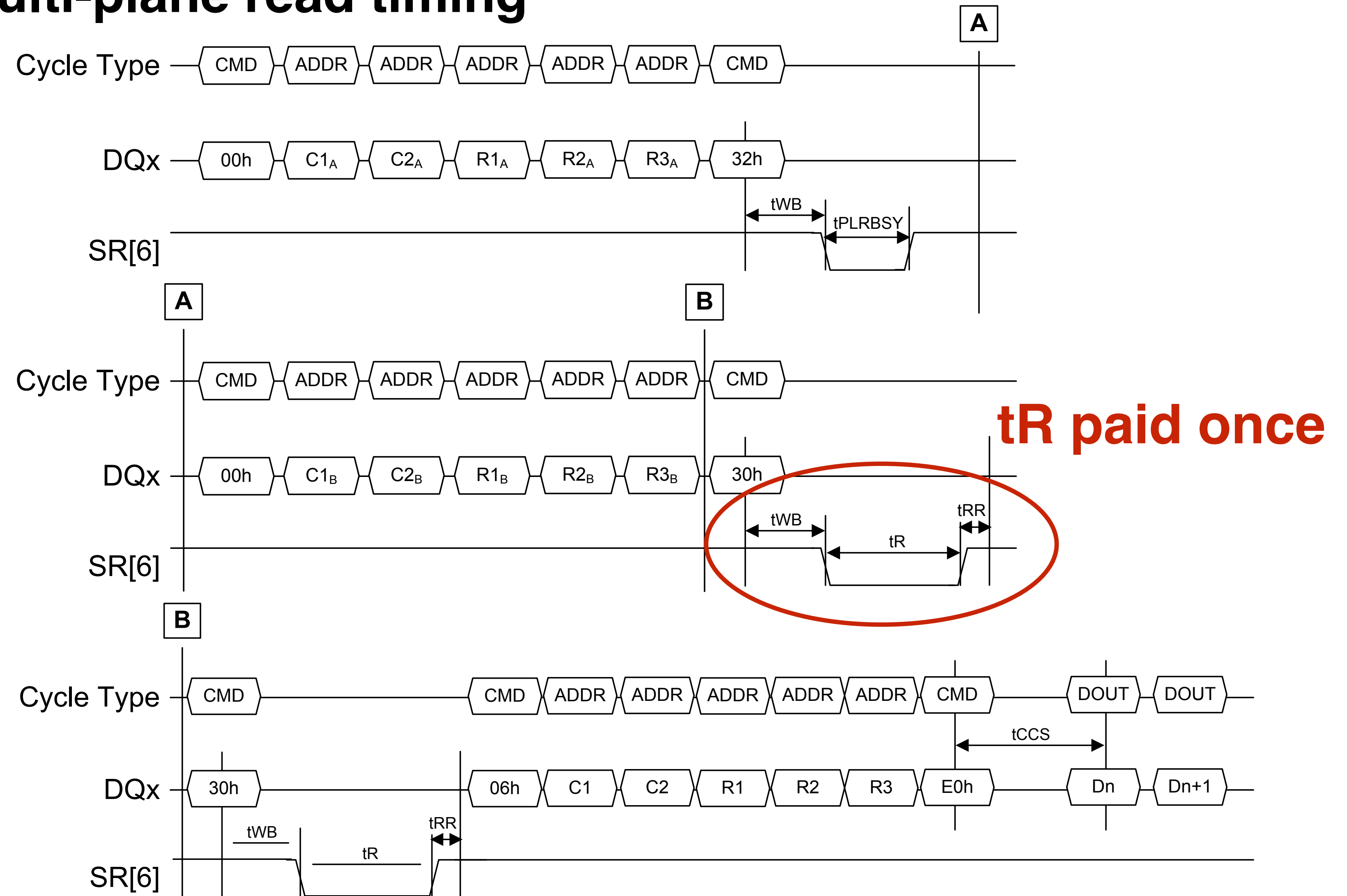
**Multi-plane Ops (Program, Copyback, Erase, Read)**

*allows parallel or staggered commands to multiple planes  
for example ...*





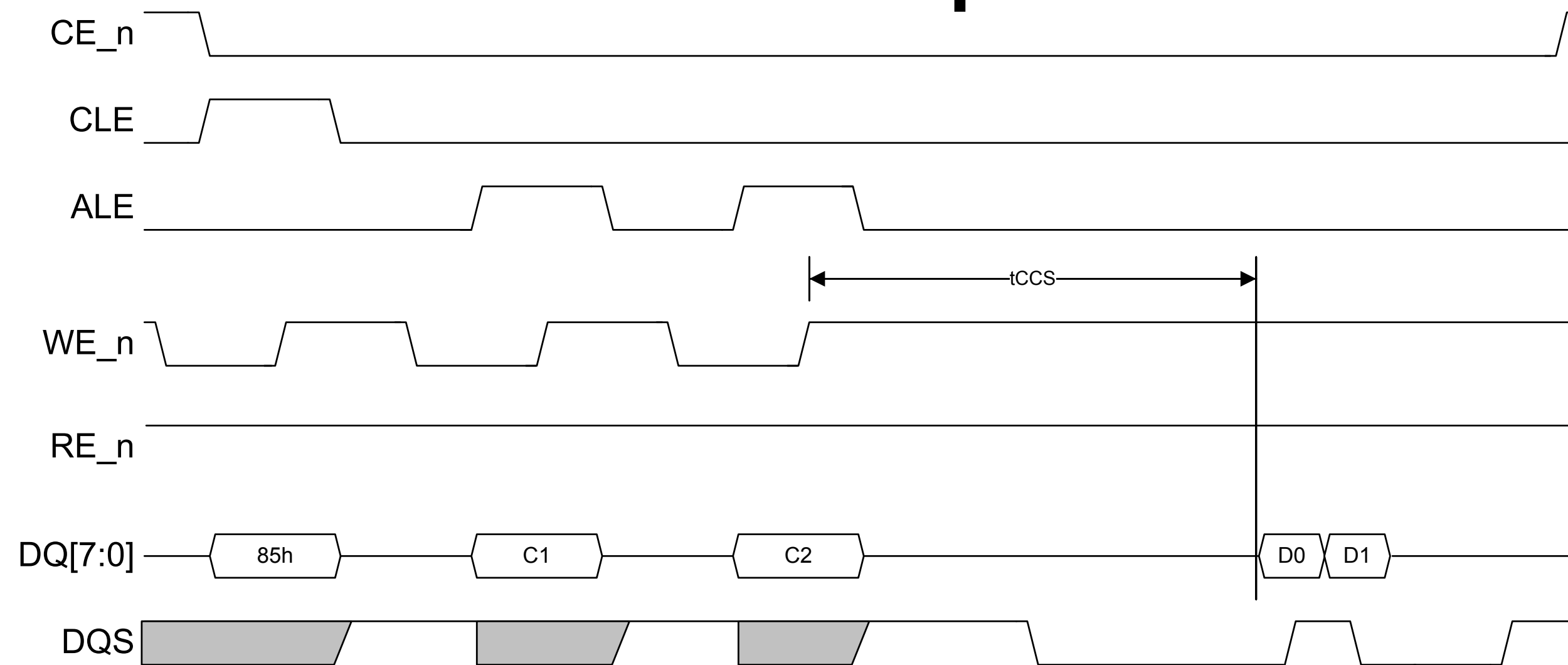
## Multi-plane read timing





## NV-DDR2 Differences

**Differential signaling (e.g., DQS\_t and DQS\_c) & ODT  
CLK not used for command capture:**



**Optional Data Warm-up Cycles:**

