NAND Flash memory

Samsung Electronics, co., Ltd

Flash design team

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- Flash memory 101
- Basic operations
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- In the near future

NAND Flash Application

“Flash memory” in Wikipedia

- Flash memory is a non-volatile computer storage technology that can be electrically erased and reprogrammed.
- Flash memory offers fast read access times (although not as fast as volatile DRAM memory used for main memory in PCs) and better kinetic shock resistance than hard disks.
- Flash memory (both NOR and NAND types) was invented by Dr. Fujio Masuoka while working for Toshiba circa 1980. According to Toshiba, the name "flash" was suggested by Dr. Masuoka's colleague, Mr. Shoji Ariizumi, because the erasure process of the memory contents reminded him of the flash of a camera.
- NAND flash also uses floating-gate transistors, but they are connected in a way that resembles a NAND gate : several transistors are connected in series, and only if all word lines are pulled high (above the transistors' VT) is the bit line pulled low.

“Flash memory” in Wikipedia

- To read, most of the word lines are pulled up above the VT of a programmed bit, while one of them is pulled up to just over the VT of an erased bit. The series group will conduct (and pull the bit line low) if the selected bit has not been programmed. NAND flash uses tunnel injection for writing and tunnel release for erasing.

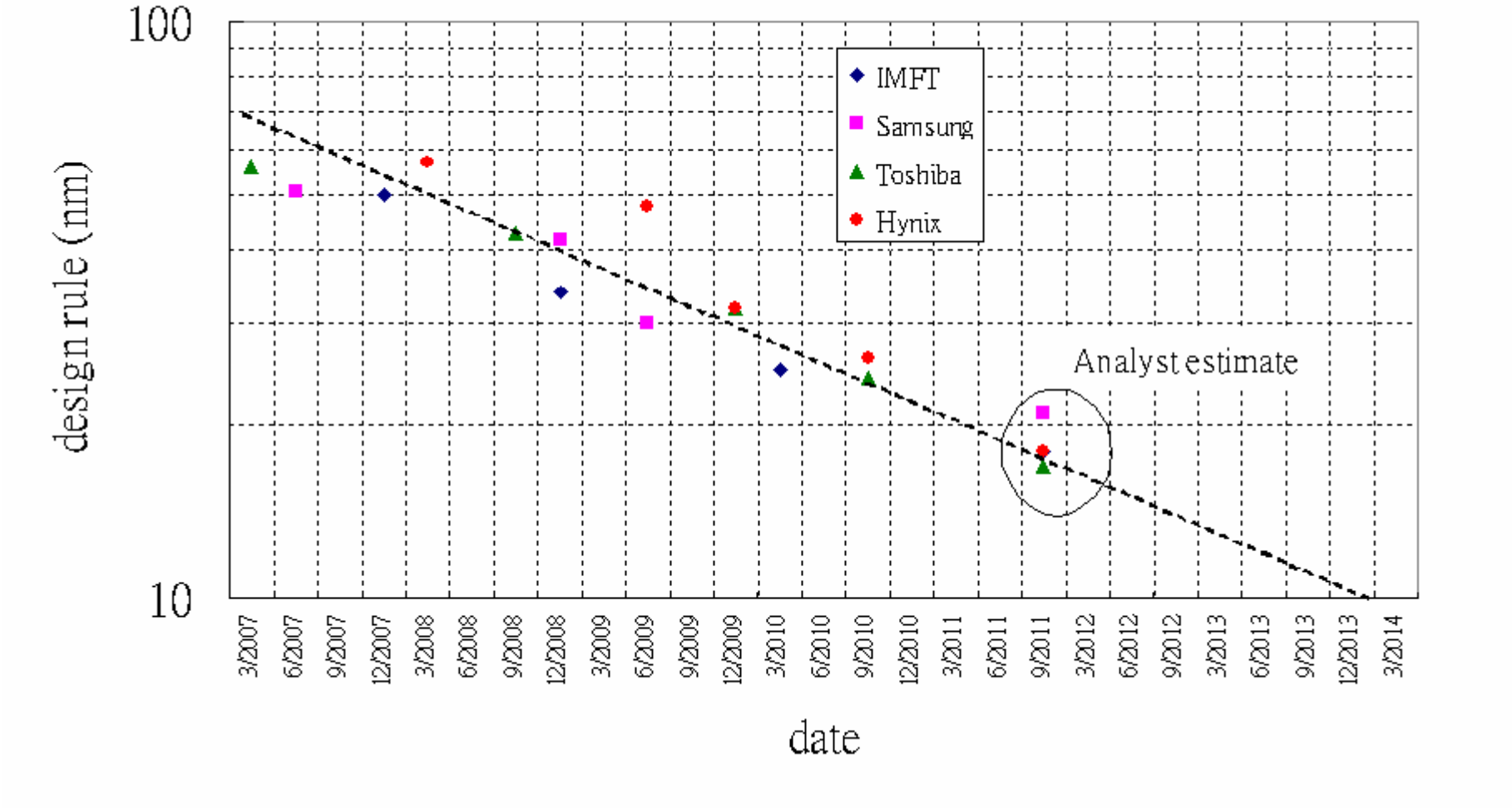
- One limitation of flash memory is that although it can be read or programmed a byte or a word at a time in a random access fashion, it must be erased a "block" at a time.

- Another limitation is that flash memory has a finite number of erase-write cycles. Most commercially available flash products are guaranteed to withstand around 100,000 write-erase-cycles, before the wear begins to deteriorate the integrity of the storage

“Flash memory” in Wikipedia

- **Technology scaling down**

Reference: EETimes article on NAND scaling, 3/22/2010



Major players

Table 4. NAND Market Share

2009	Sales ($M)	Share (%)	GB Equivalent (M)	Share (%)
Samsung	5,337	37.10	2,007	31.50
Toshiba	3,570	24.80	1,689	26.50
SanDisk	1,997	13.90	1,181	18.50
Micron	1,203	8.40	664	10.40
Hynix	1,066	7.40	347	5.40
Intel	826	5.70	465	7.30
Numonyx	330	2.30	18	0.30
Spansion	37	0.30	3	0.00
Powerchip	3	0.00	2	0.00
Renesas	2	0.00	-	0.00
Total	**14,371**	**100**	**6,375**	**100**

Source: Gartner (March 2010)

Now in the market …

Intel, Micron and IMFT announce world's first 25-nm NAND technology

February 2, 2010, By Sanjeev Ramachandran in Hardware

The NAND flash production scene has received a shot in the arm with Intel Corporation and Micron Technology making it public that the world's first 25-nanometer (nm) NAND technology is now on stream. Significantly enough, the 25nm process is the smallest NAND technology as well as the smallest semiconductor technology in the world

Hynix Develops 26nm NAND Flash Memory

Tuesday, February 09, 2010

South Korea's Hynix Semiconductor Inc., the world's second-largest memory chipmaker, said Tuesday that it has developed a 26-nanometer based NAND flash memory chip. The company is the world's second flash memory maker to apply the below 30-nanometer technology. Mass production of the new memory will start in in July.

Toshiba readies sub-25nm flash memory chip production

By Jose Vilches, TechSpot.com Published: April 5, 2010, 12:14 PM EST

The company produces 32nm and 43nm memory chips, but the plan is to begin production on "sub-25nm" chips that would enable larger storage capacities to be shoved into the same form factors that we use today. Toshiba will begin output of NAND chips with circuitry widths in the upper 20 nanometre range soon, while production of chips with circuitry widths in the lower 20 nanometres is slated to start as early as 2012.

Samsung pioneers 20-nm NAND flash memory technology

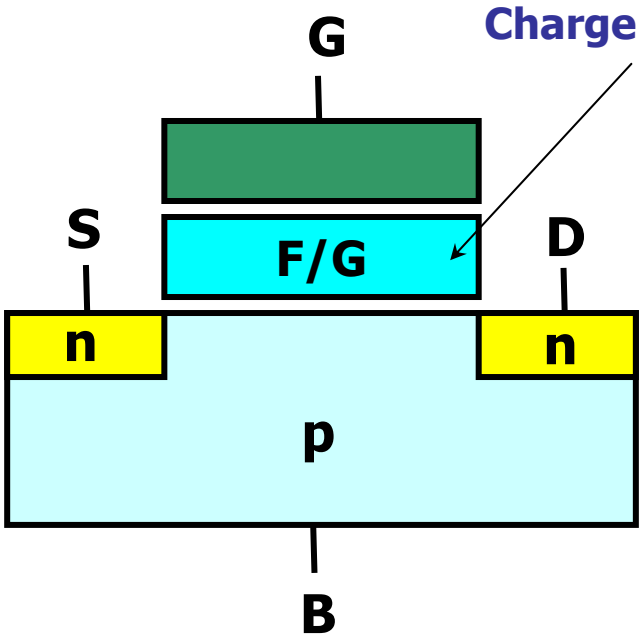
April 19, 2010, By Thomas Antony in Storage

Right on the heels of Toshiba's announcement to start on sub-25nm flash memory, Samsung today announced the industry's first production of 20 nanometer class NAND chips for use in SD cards. Samsung's 20nm MLC 32-gigabit NAND chips are sampling now for use in embedded storage and SD memory cards ranging from 4GB to 64GB. This is a significant step forward for Samsung who started its 30nm production just one year ago. The new class of memory chips will allow for higher-density in storage, lower manufacturing costs and 50% higher productivity than 30nm technology.

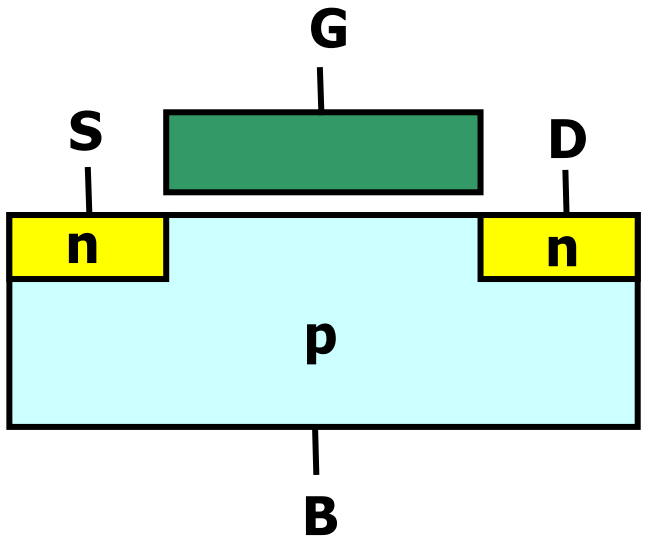
Flash memory 101

Flash memory cell vs. MOSFET

- Flash cell has a charge storage layer such that Vth of a cell can be changed → memorize information



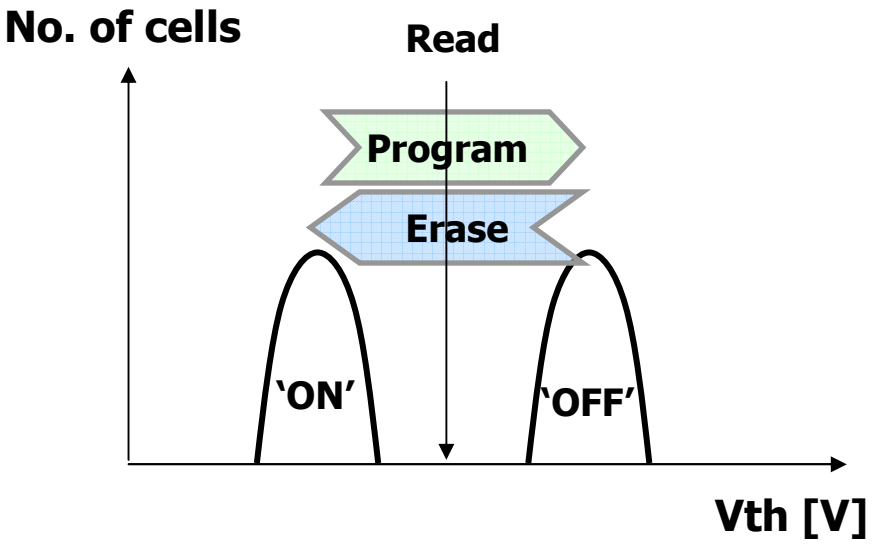
Flash cell

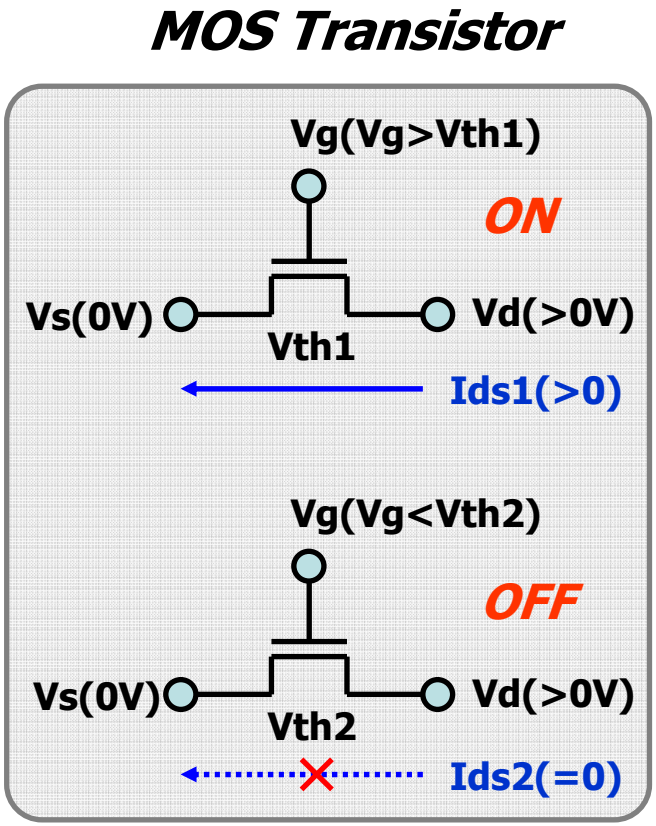


MOSFET

Flash memory operation

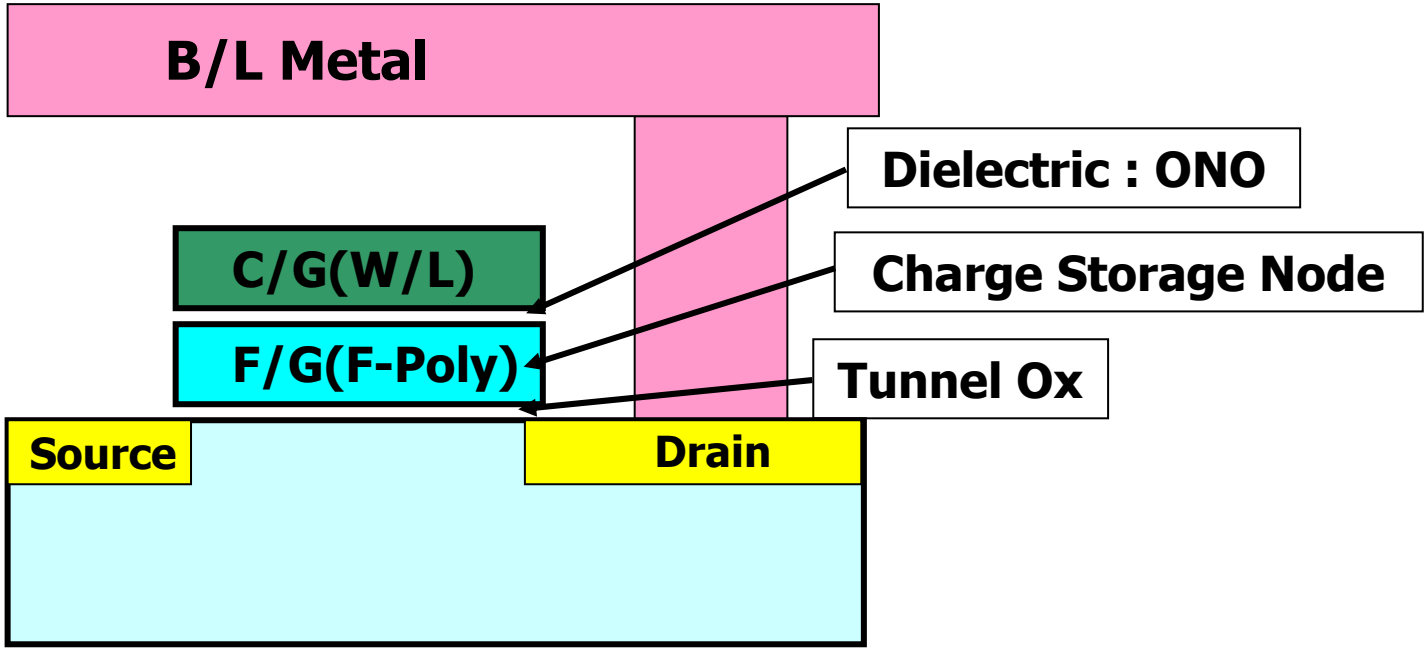
- **Write & read binary data to a flash cell**
  - data '0' → 'OFF' state (program)
  - data '1' → 'ON' state (erase)





Flash memory cell structure

- Cell Vth changes depending on the amount of F/G charge
- electrons can be injected(ejected) into(out of) the F/G through Tox with electric field across Tox



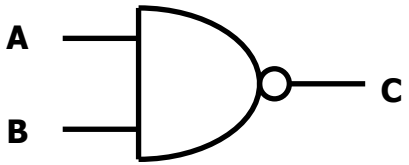
NAND vs. NOR

NAND

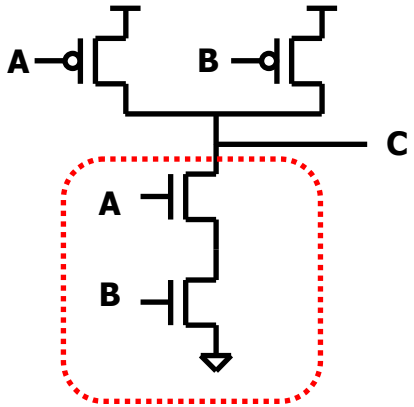
Truth table

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Logic gate



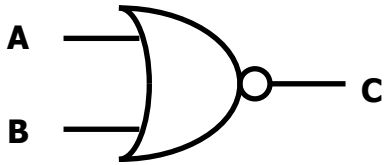
circuit

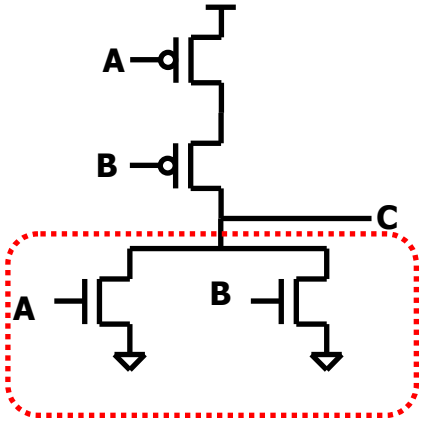


Flash

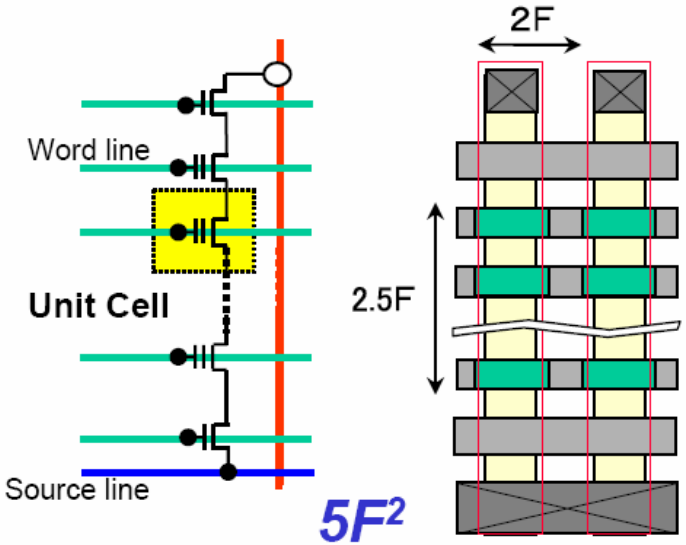
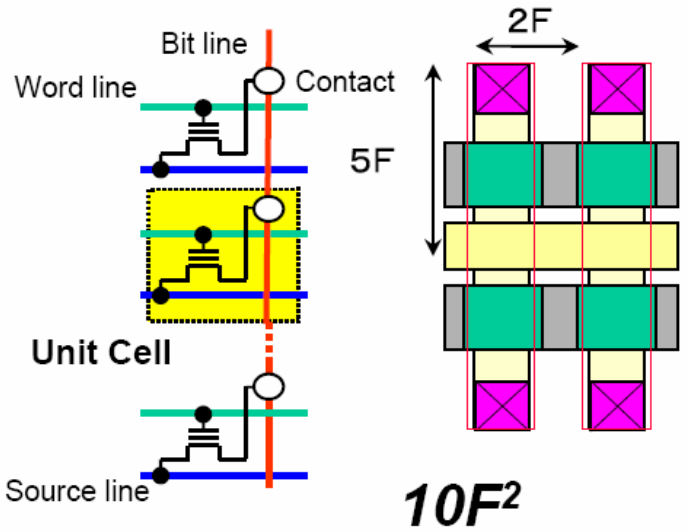
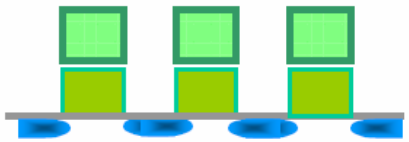
NOR

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0



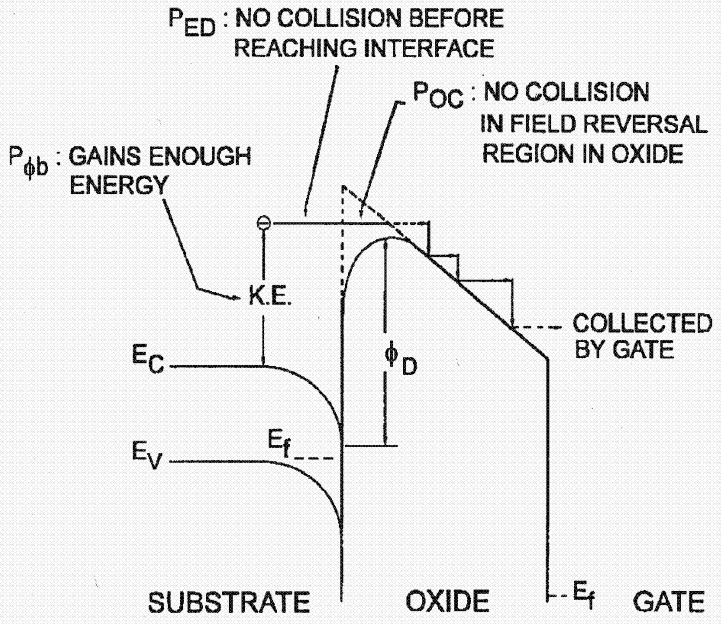


Features : NAND vs. NOR

	NAND	NOR
Cell Array & Size		
Cross-section		
Features	Small Cell Size, High Density Low Power & Good Endurance ➔ *Mass Storage*	Large Cell Current, Fast Random Access ➔ *Code Storage*

Write methods in Flash memory

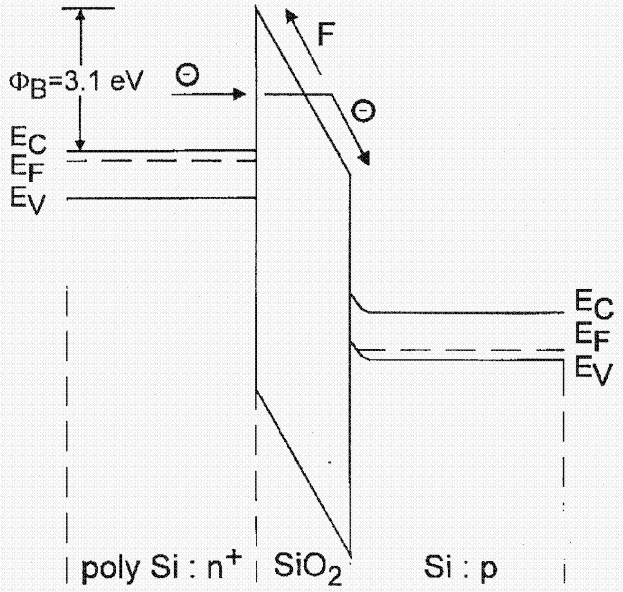
Hot Electron Injection



Program in NOR Flash

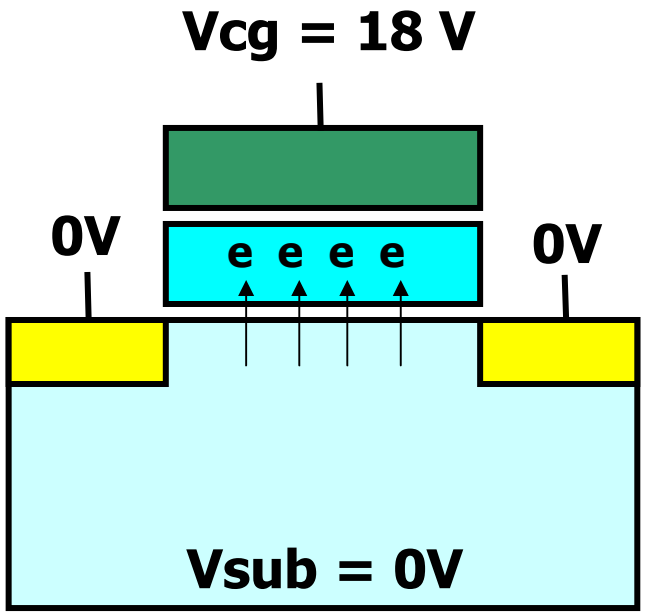
Impact ionization at drain side

Fowler-Nordheim Tunneling



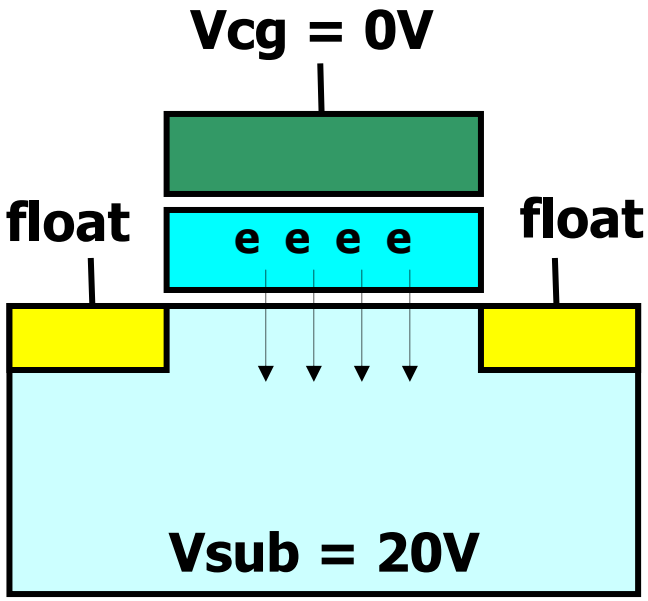
Program/Erase in NAND Flash
Erase in NOR Flash

NAND Flash : Program & Erase



Program
F-N Tunneling

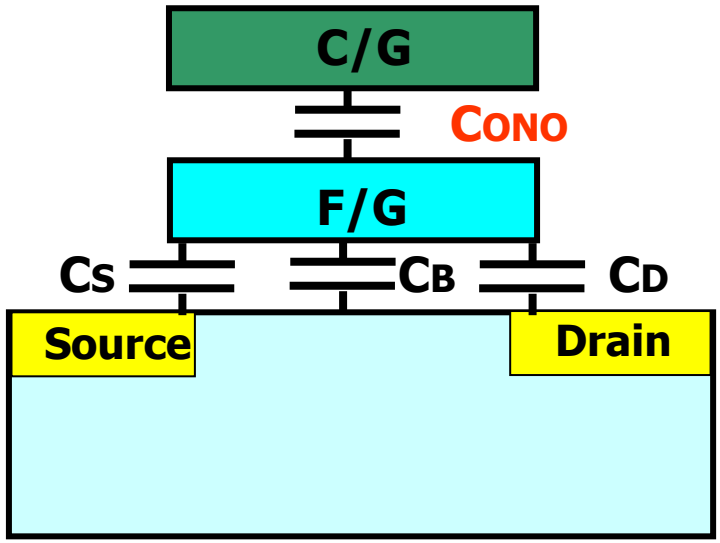
Off cell
(Solid-0)



Erase
F-N Tunneling

On cell
(Solid-1)

Coupling ratio



$$Vfg = Vcg \times \alpha_{cg}$$

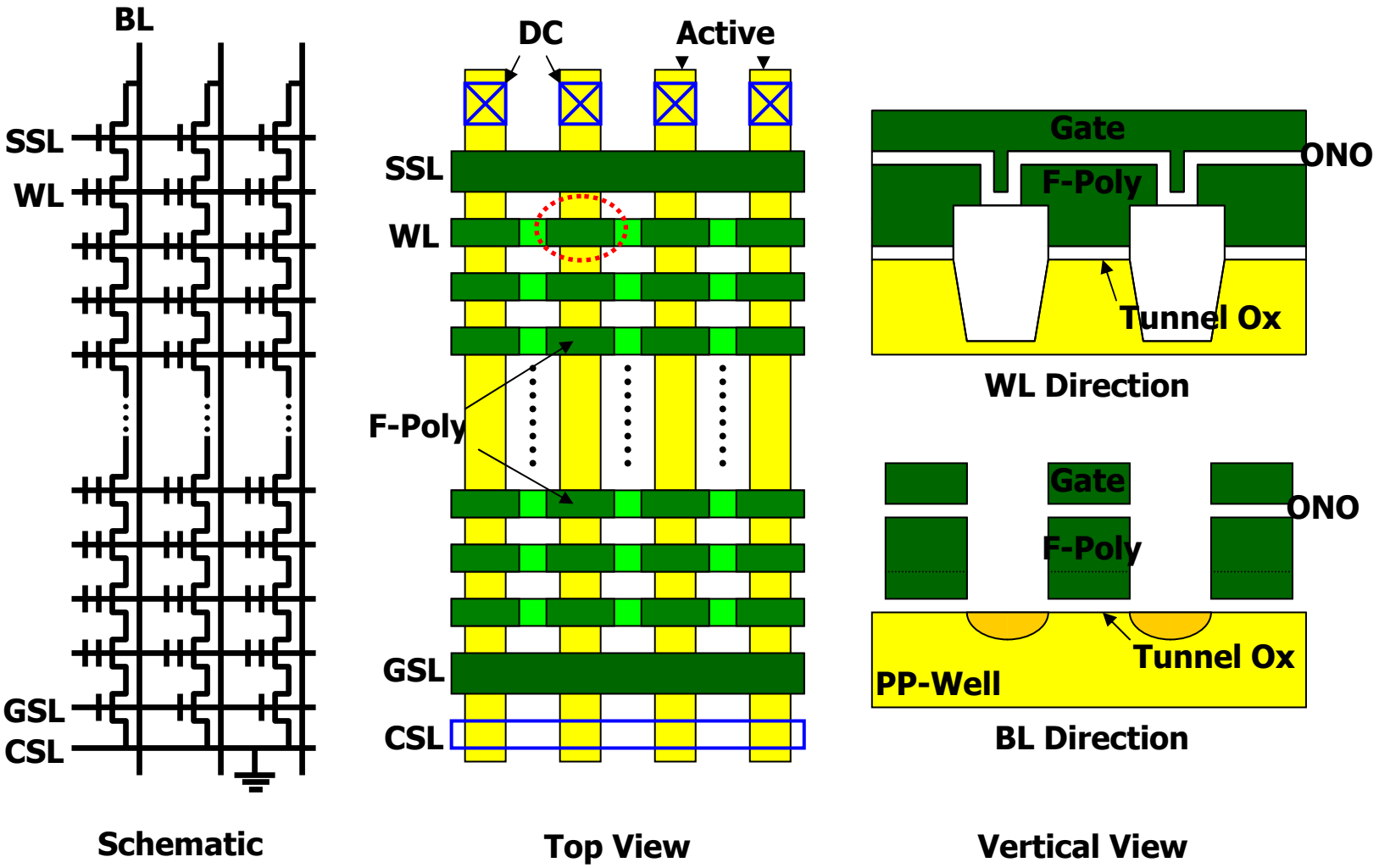
$$\alpha_{cg} = \frac{C_{ONO}}{(C_D + C_S + C_B + C_{ONO})}$$

α_{cg} : Coupling Ratio

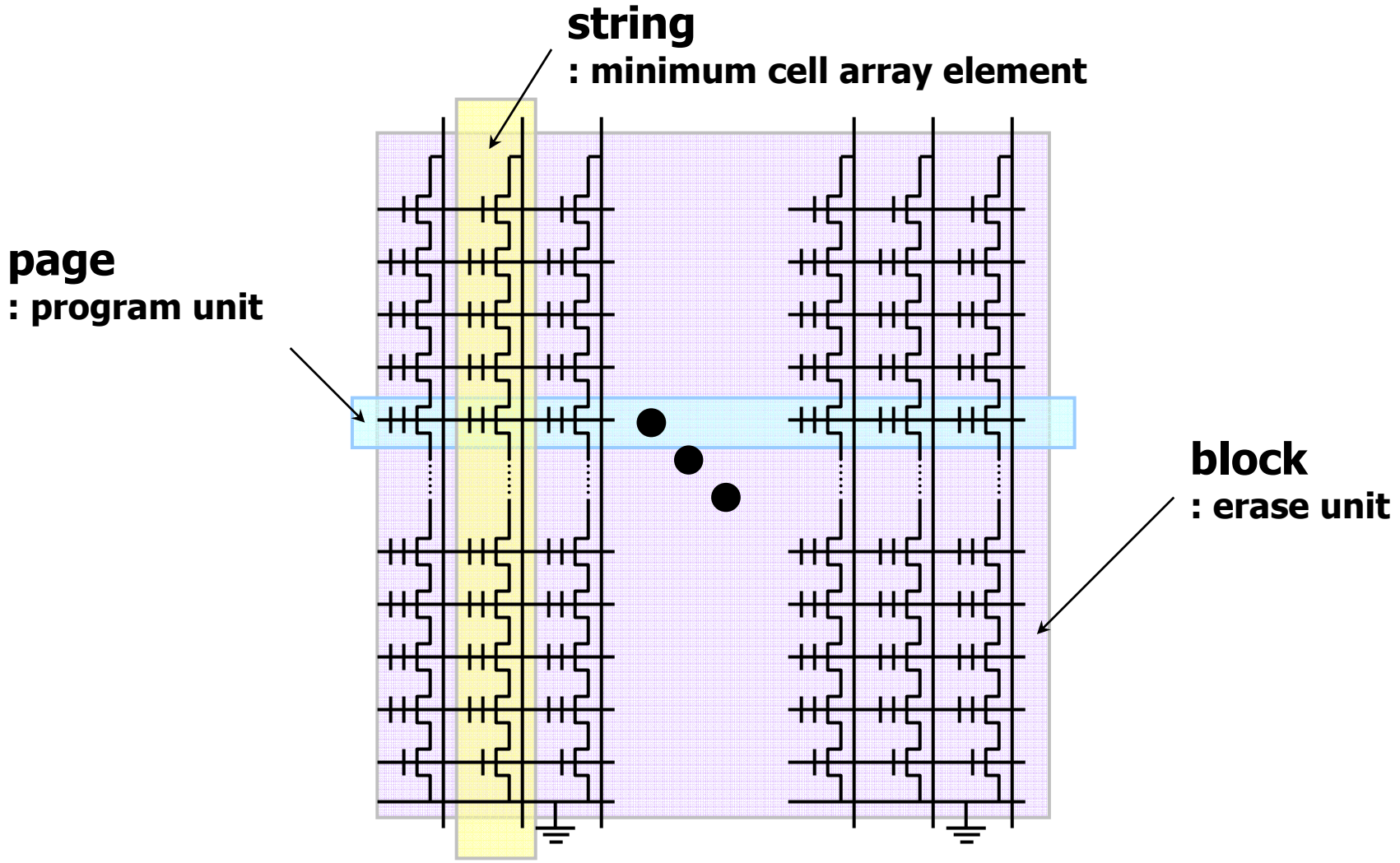
(From Q=CV and
Charge Conservation Law)

For fast programming, high Vfg is required,
i.e. either high Vcg or large α_{cg}

NAND Flash cell structure

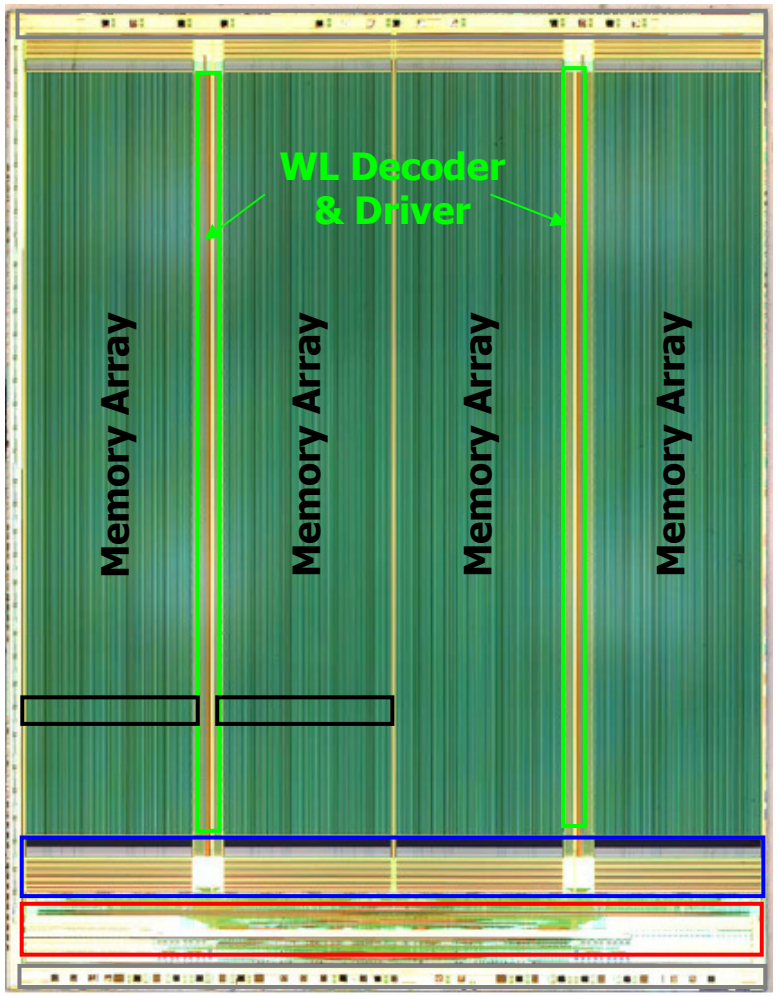


Terms in NAND Flash – string, page, block



NAND Flash chip architecture

- **High density & simple architecture (cell efficiency > 65%)**



Control I/O Pad

Block
= 128-page
(2Mb~4Mb)

SLC : 64-page
MLC : 128-page

Page Driver & Buffer (2KB~4KB)

Peripheral & Charge Pump

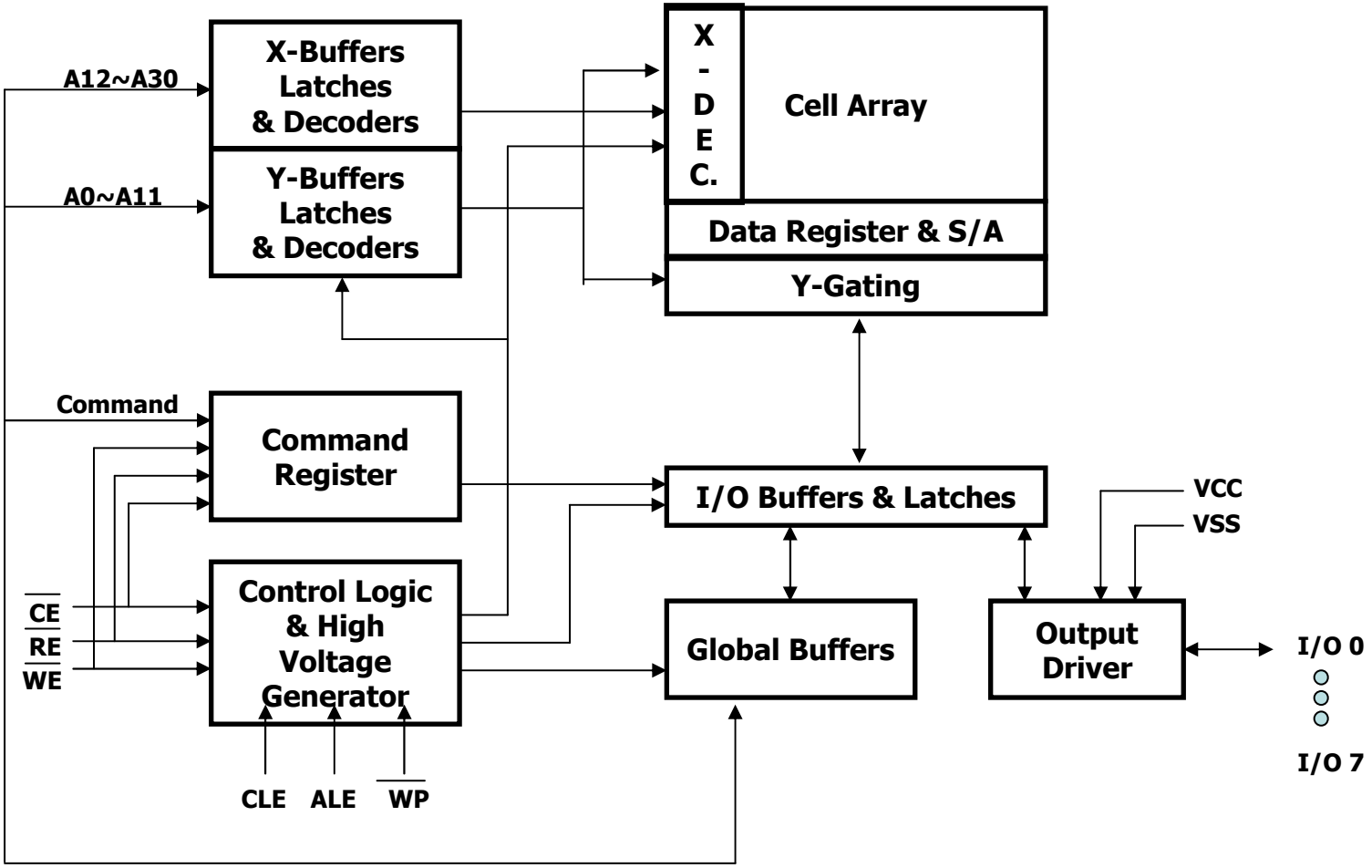
Data I/O Pad

Samsung 63nm 8Gb MLC NAND

POSTECH

SAMSUNG ELECTRONICS

Functional block diagram of NAND Flash

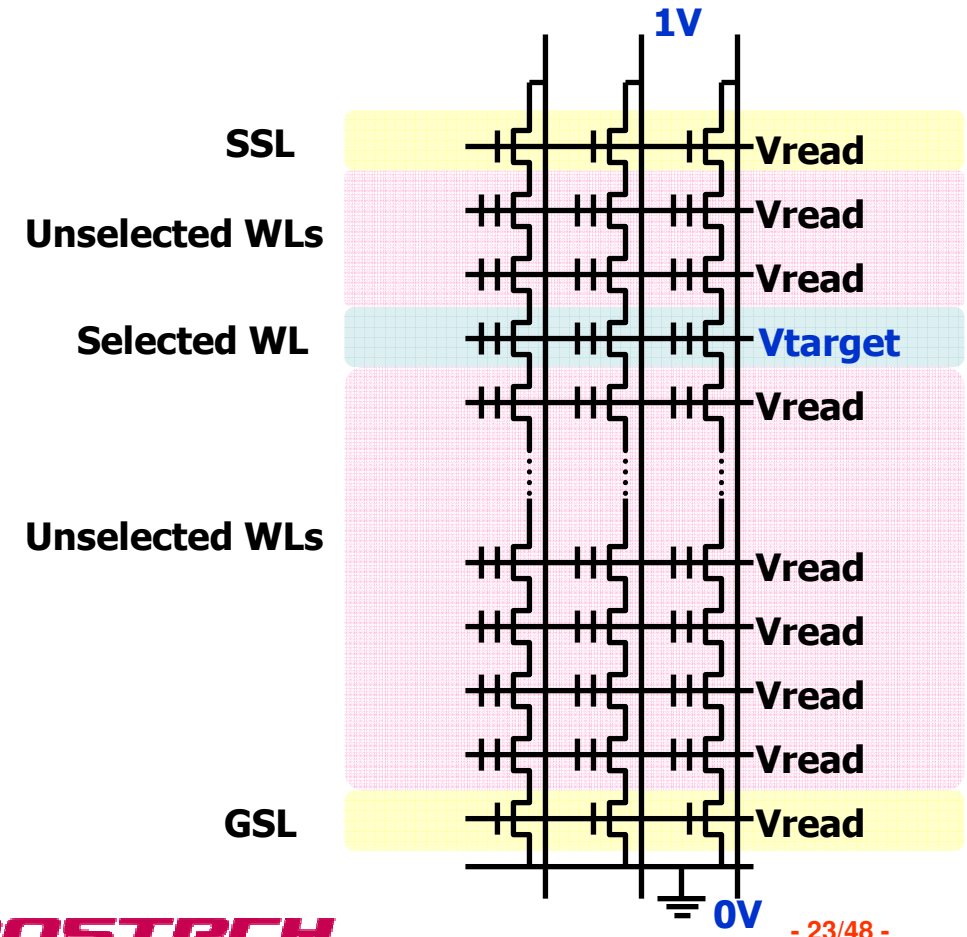


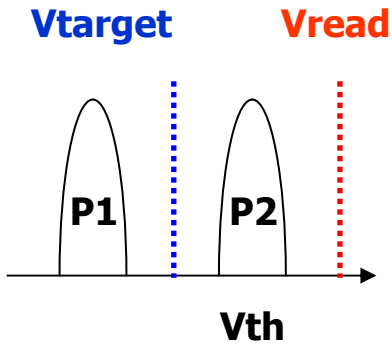
Basic operations

NAND Flash

Read operation

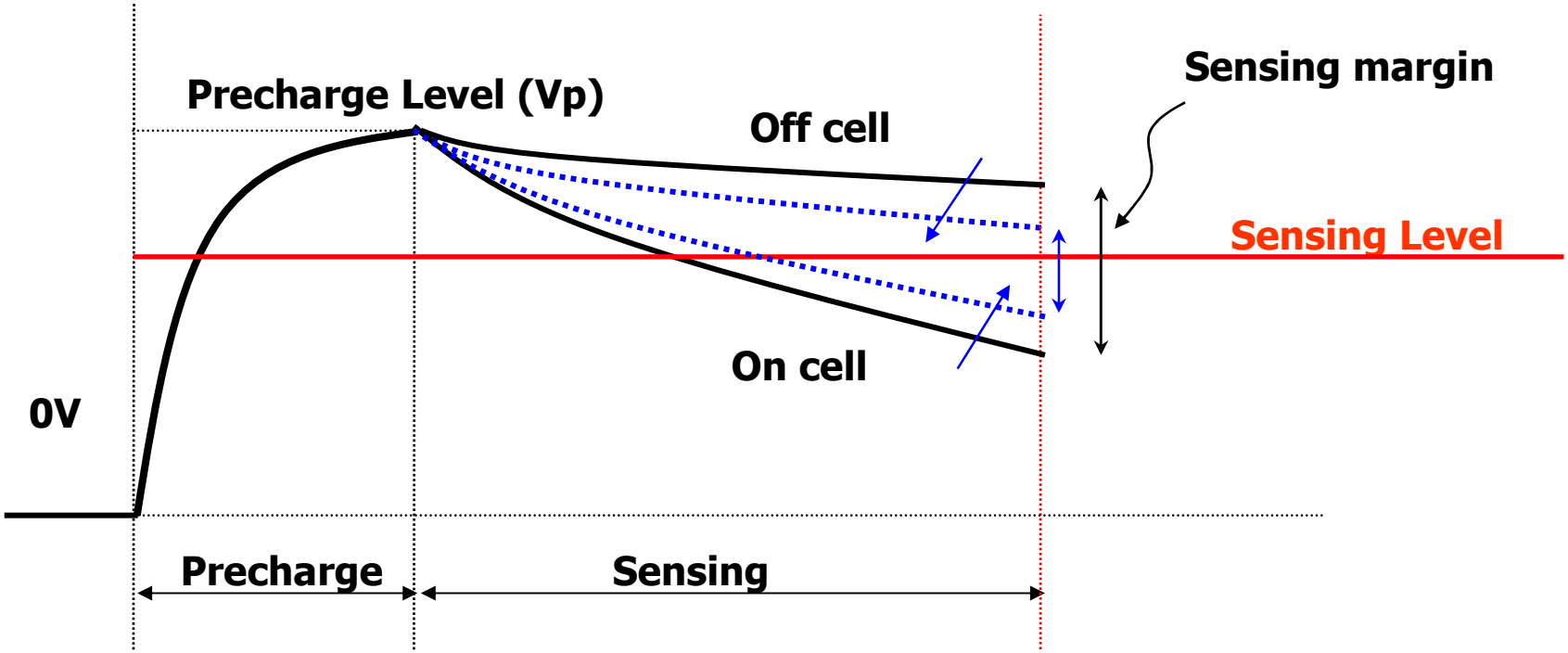
- **Bias condition**
  - selected WL : Target voltage (Vtarget)
  - unselected WLs : high enough to conduct all cells in a string





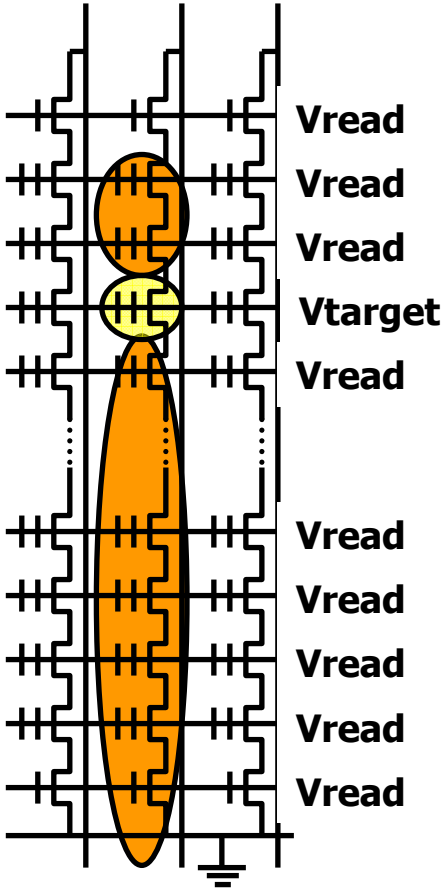
Sensing margin

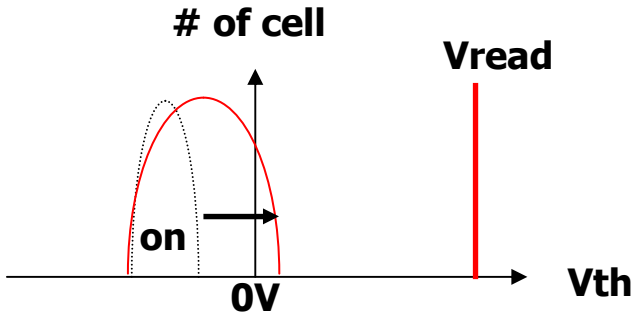
- The ratio of On cell & Off cell current



Read disturbance

- Increasing Vread → soft program occurs in the unselected cell of selected string

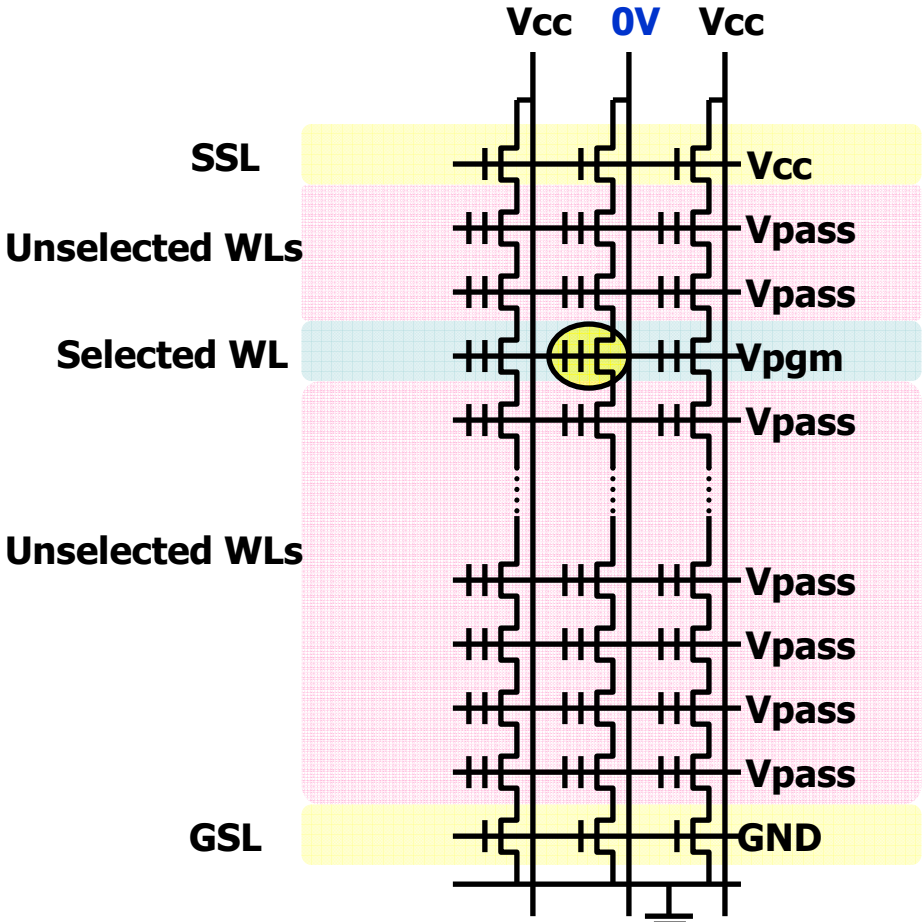


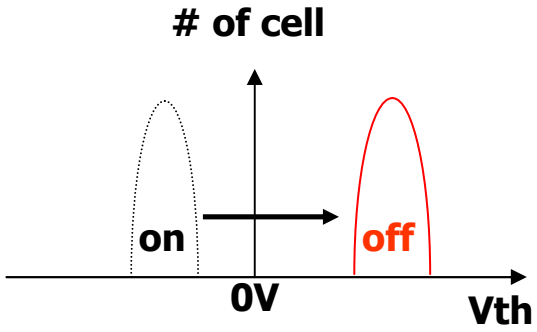


On cell moves to off cell

Program operation

- **Bias condition**
  - selected WL : Program voltage (Vpgm)
  - unselected WLs : Pass voltage (Vpass)

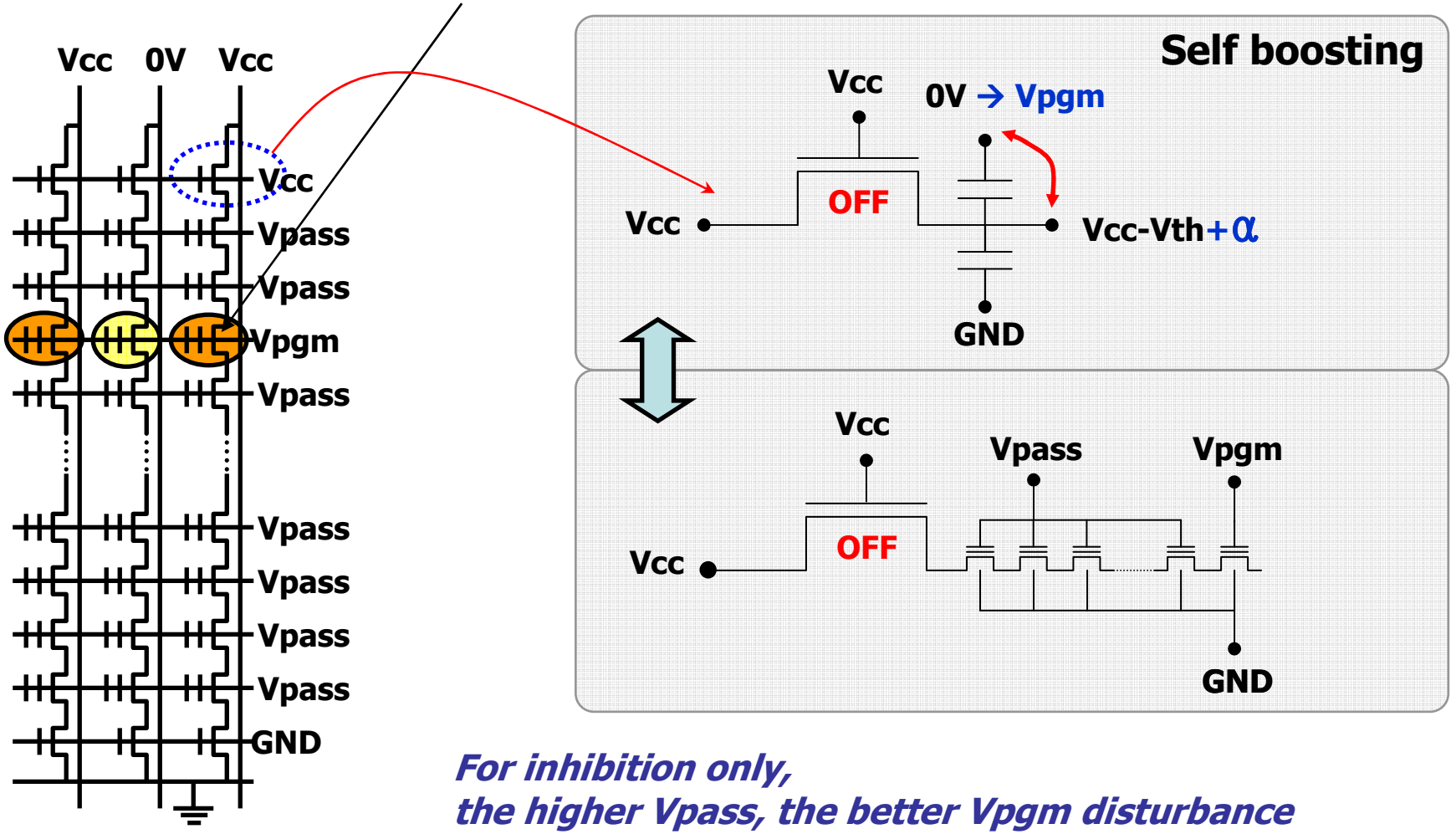




on cell becomes off cell

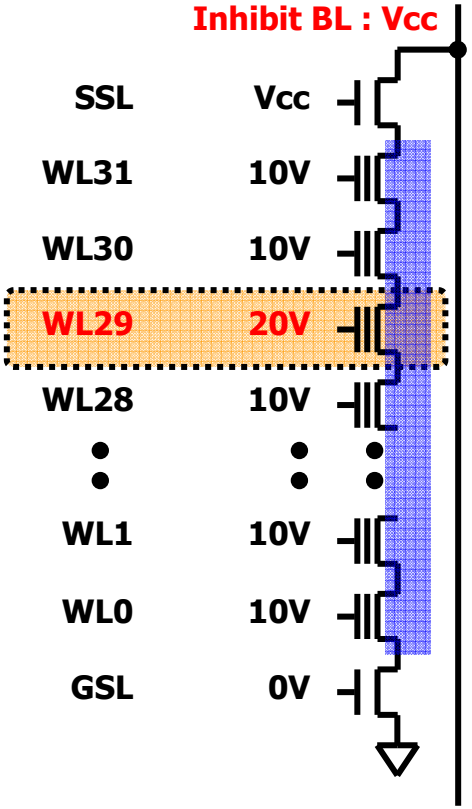
Program inhibition

Should not be programmed (= program inhibited)

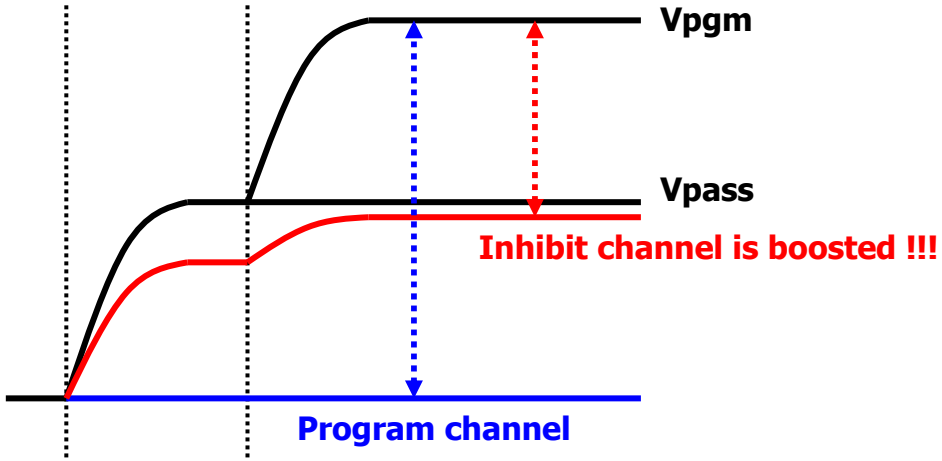


For inhibition only,
the higher Vpass, the better Vpgm disturbance
But, higher Vpass causes more Vpass disturbance

Self boosting



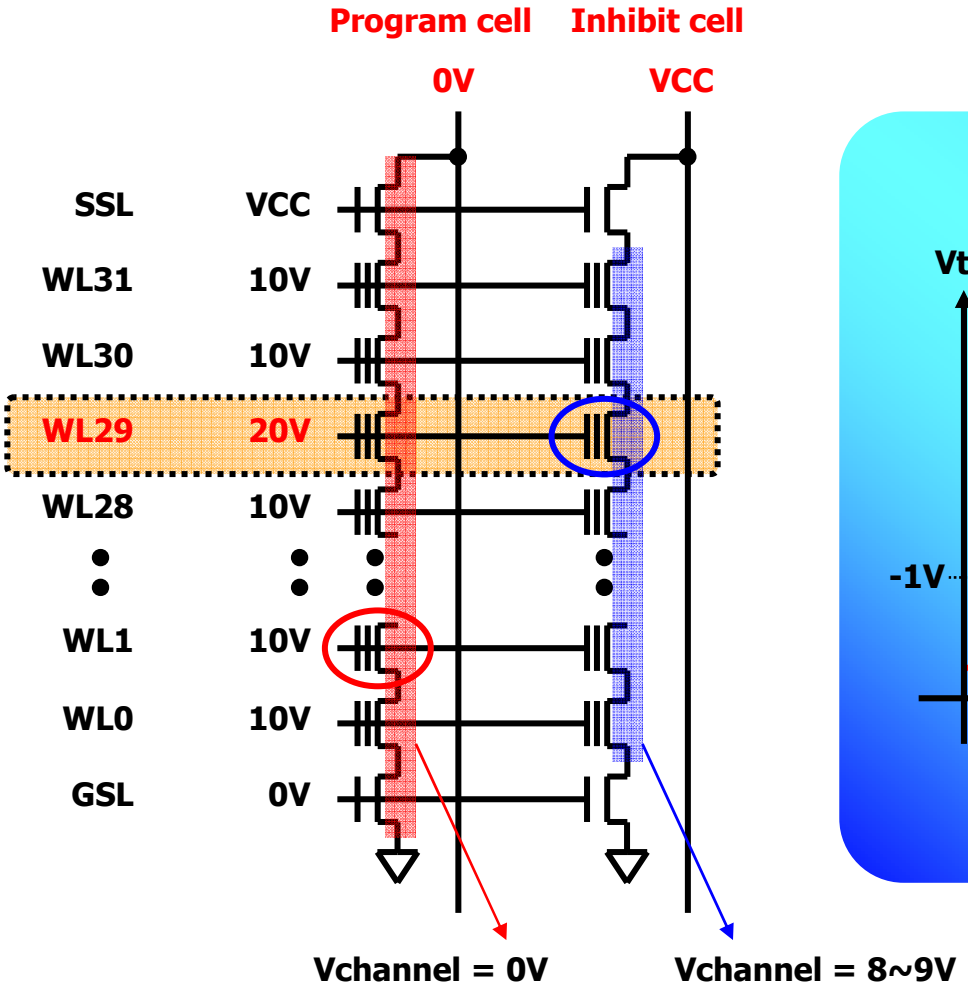
Bias sequence for self boosting

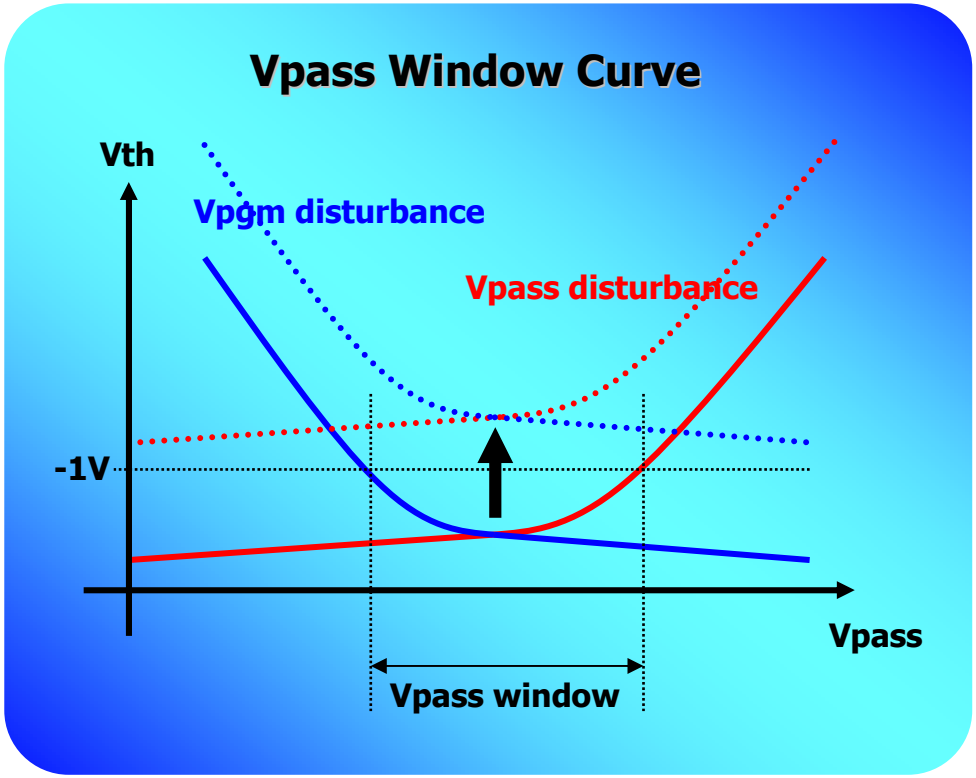


Channel potential strongly depends on the cell states in a string

Vpass window

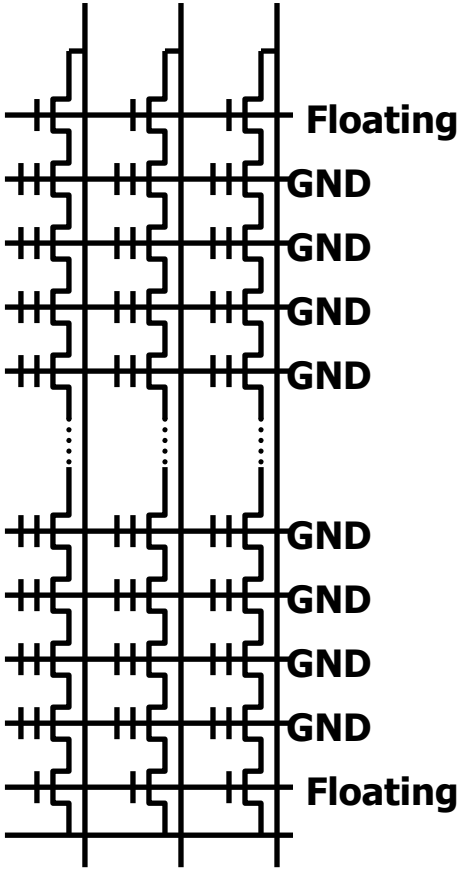
- "Optimal Vpass region" considering both Vpgm and Vpass disturbances at the same time

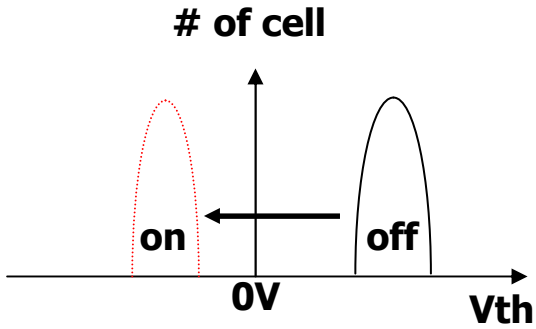




Erase operation

- **Bias condition**
  - **all WLs in the selected Block : 0V**
  - **GSL/SSL : Floating**
  - **Bulk : Vera**

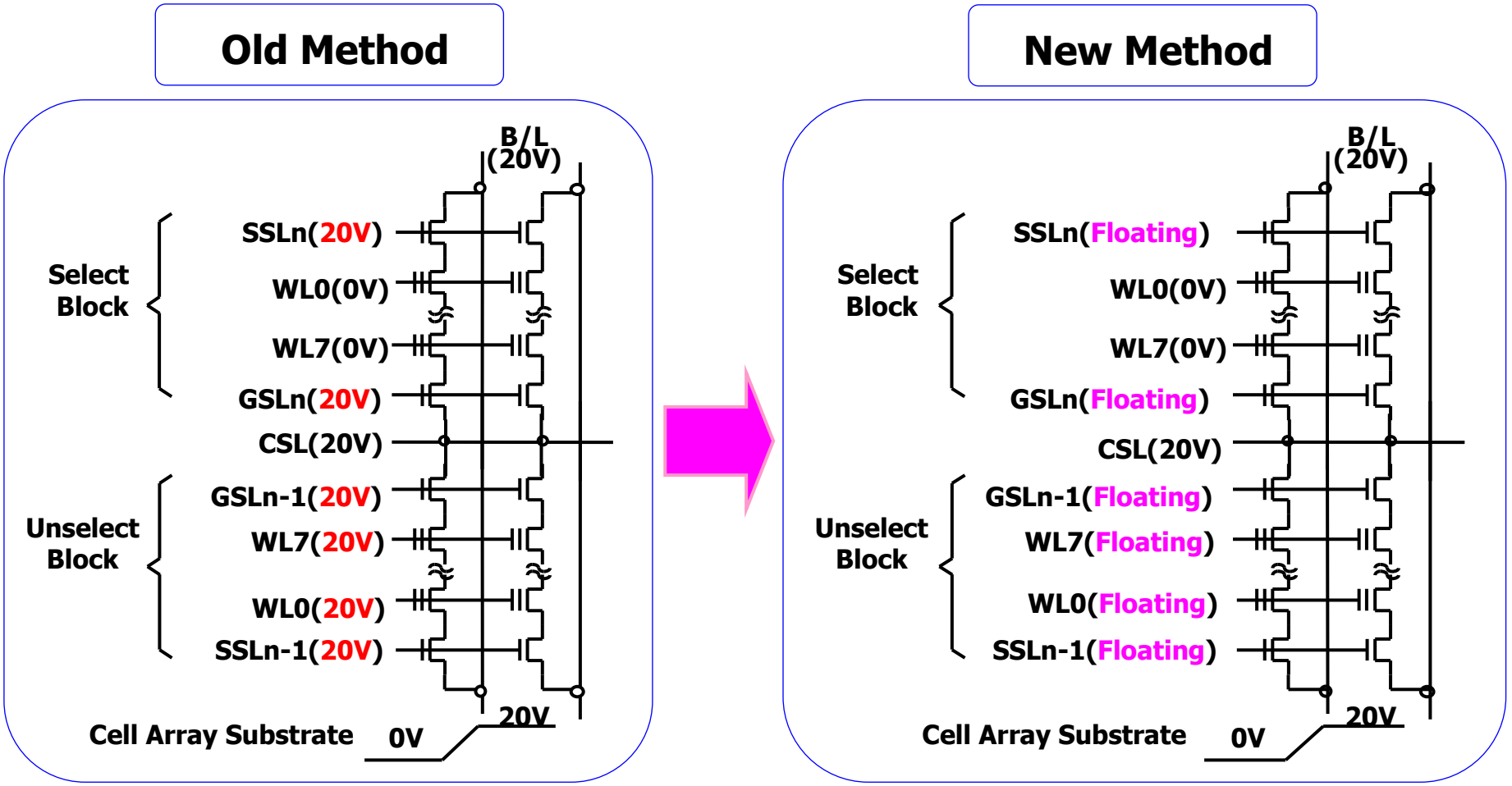




off cell becomes on cell

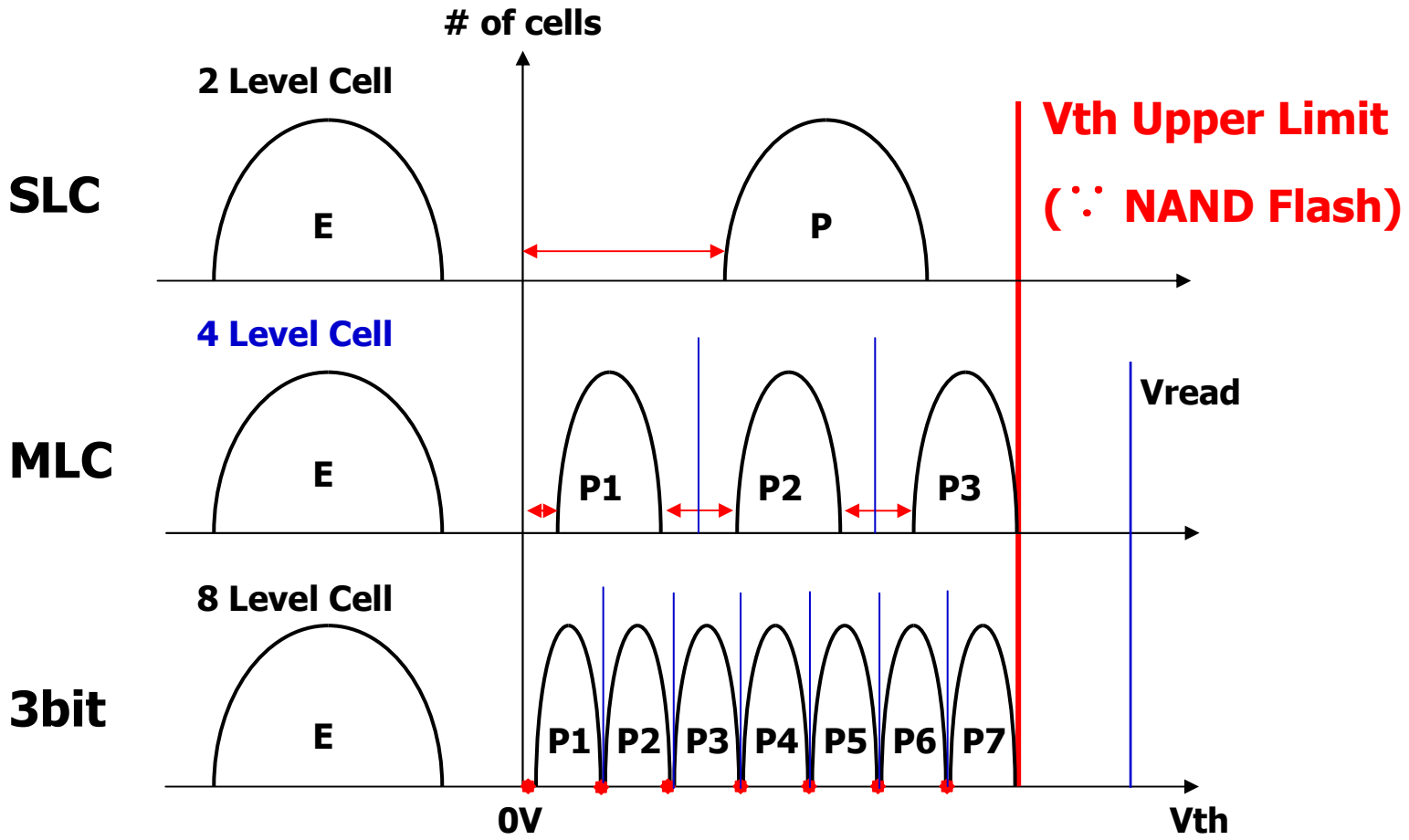
Erase disturbance

- "Self boosting" can be used



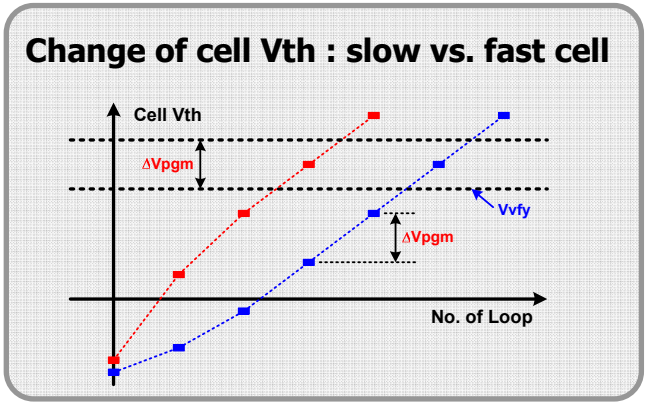
Cell Vth distribution

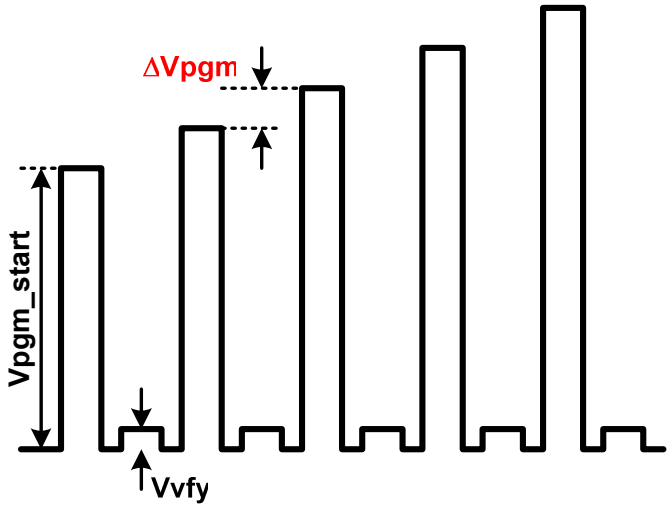
- **Cell Vth width requirement**
  - 1bit/cell vs. 2bit/cell vs. 3bit/cell

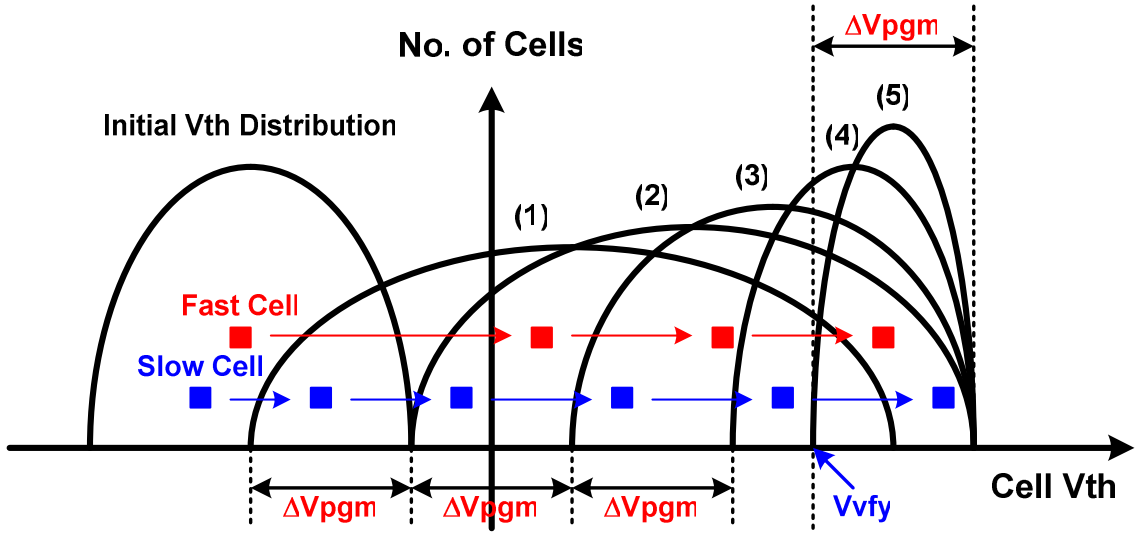


Cell Vth width control

- **Incremental Step Pulse Program (ISPP)**
  - programmed state Vth width can be controlled
  - narrower width requires more program loop

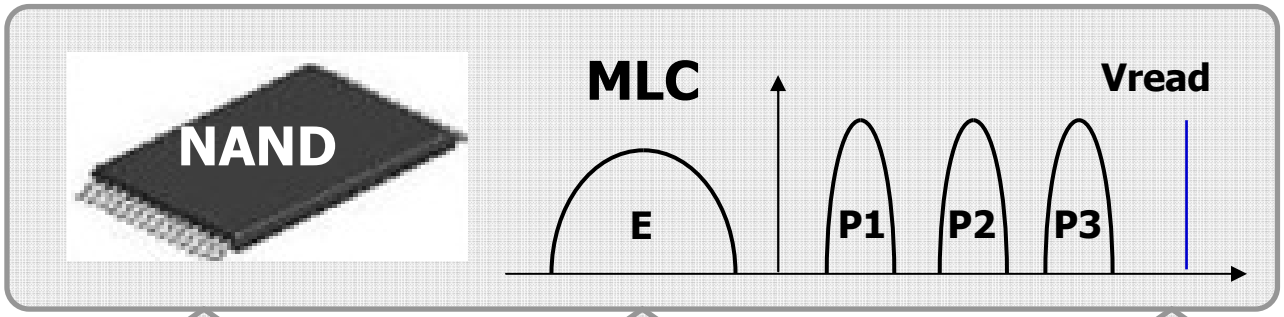






Current issues & approaches

Criteria for a NAND Flash device



Cost
- Chip size
- Bit density
- etc…

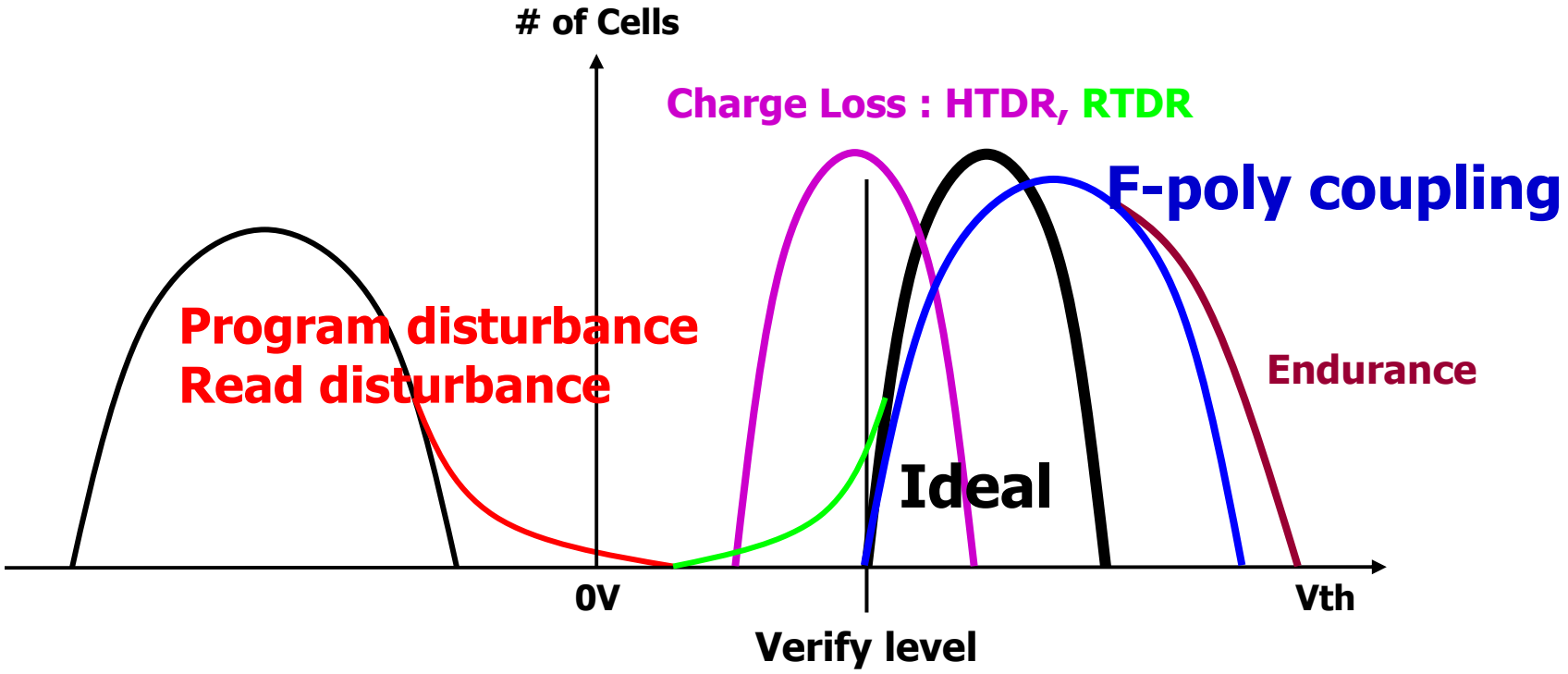
Performance
- Program time
- Read time
- etc…

Reliability
- Data retention
- Program/Read cycle
- etc…

All these are strongly dependent on each other and may become worse as "cell size shrinks down"

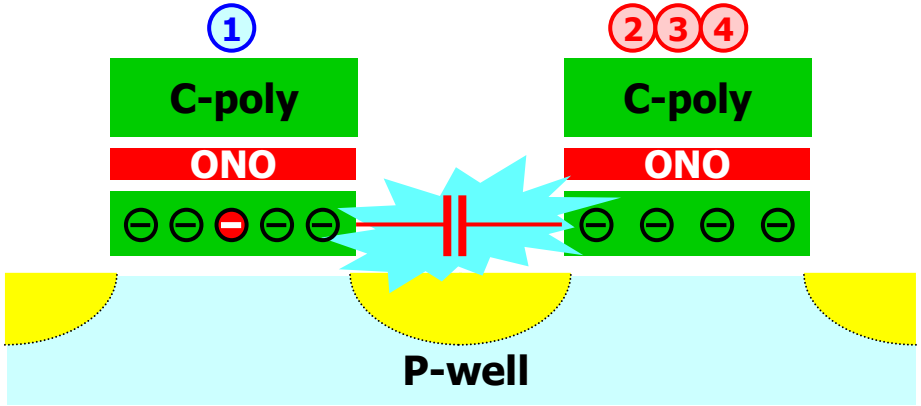
Details on programmed Vth

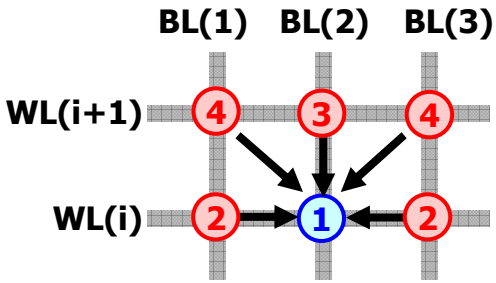
- **Factors which affect to programmed Vth width**
  - **Ideal : ⊿Vpgm during ISPP program**
  - **Noise : F-poly coupling, CSL noise, Back pattern dependency**
  - **Reliability : Endurance, program/read disturbance, charge loss**

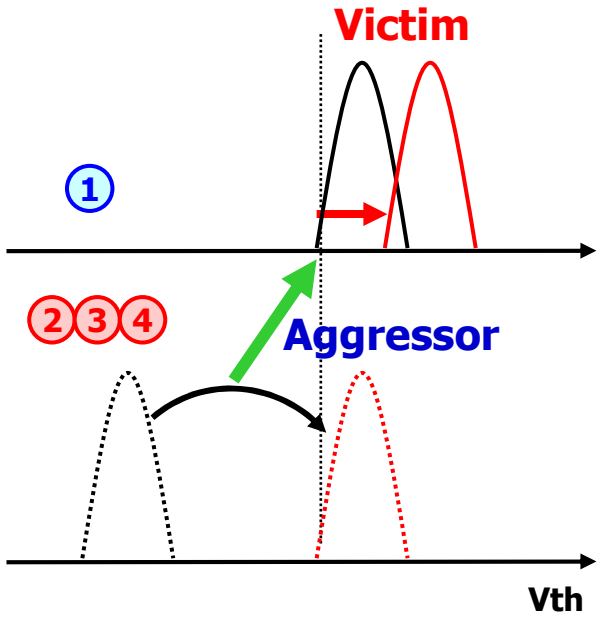


Neighborhood interference

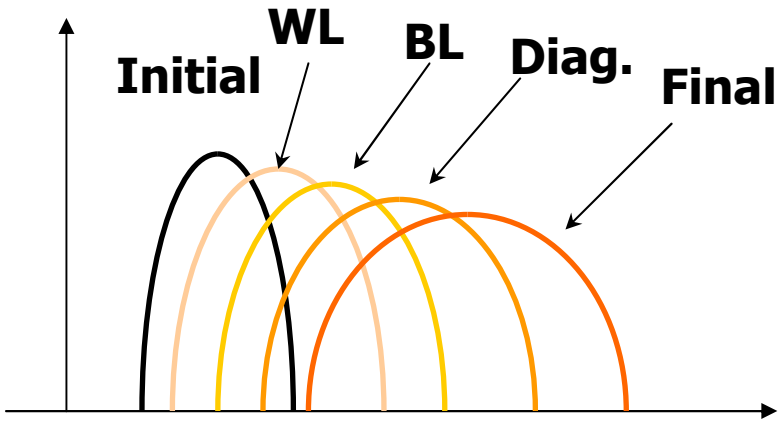
- **F-poly coupling noise**
  - **Cell Vth can be raised as neighboring cells are programmed**

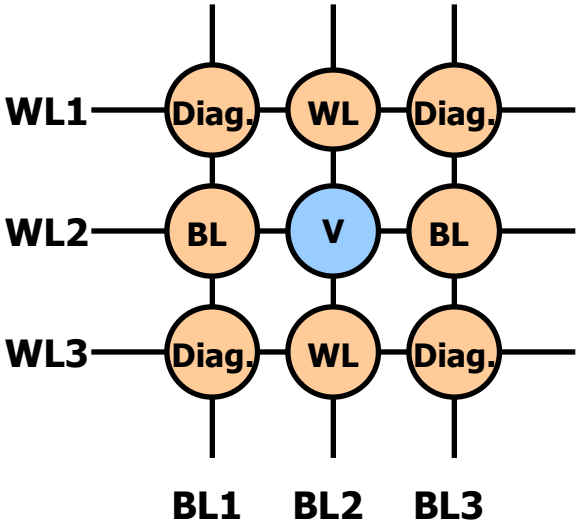


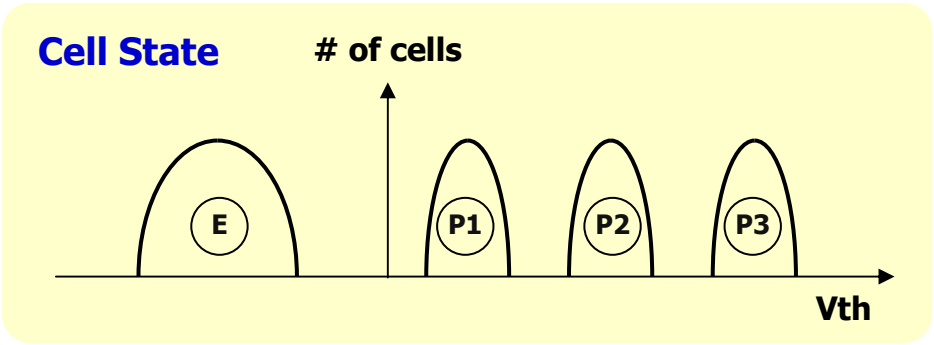




Cell Vth vs. F-poly coupling

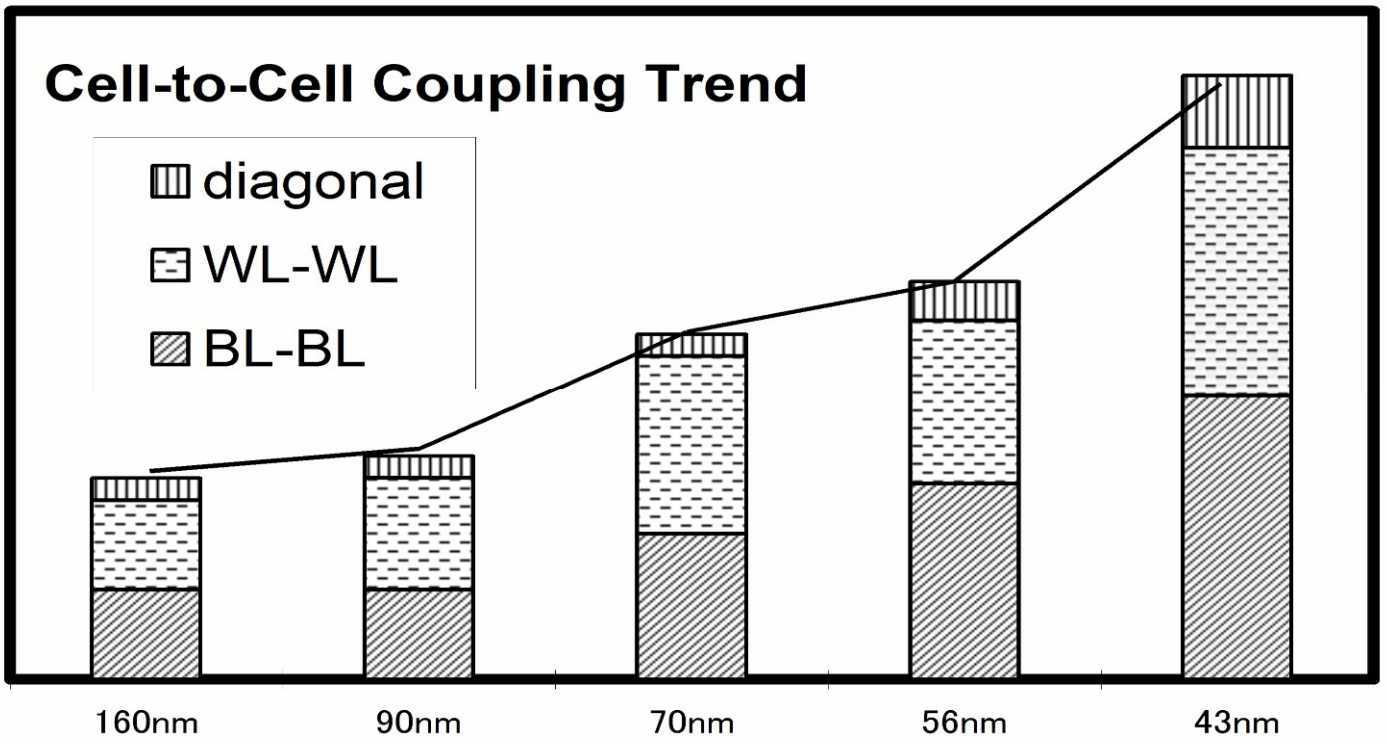






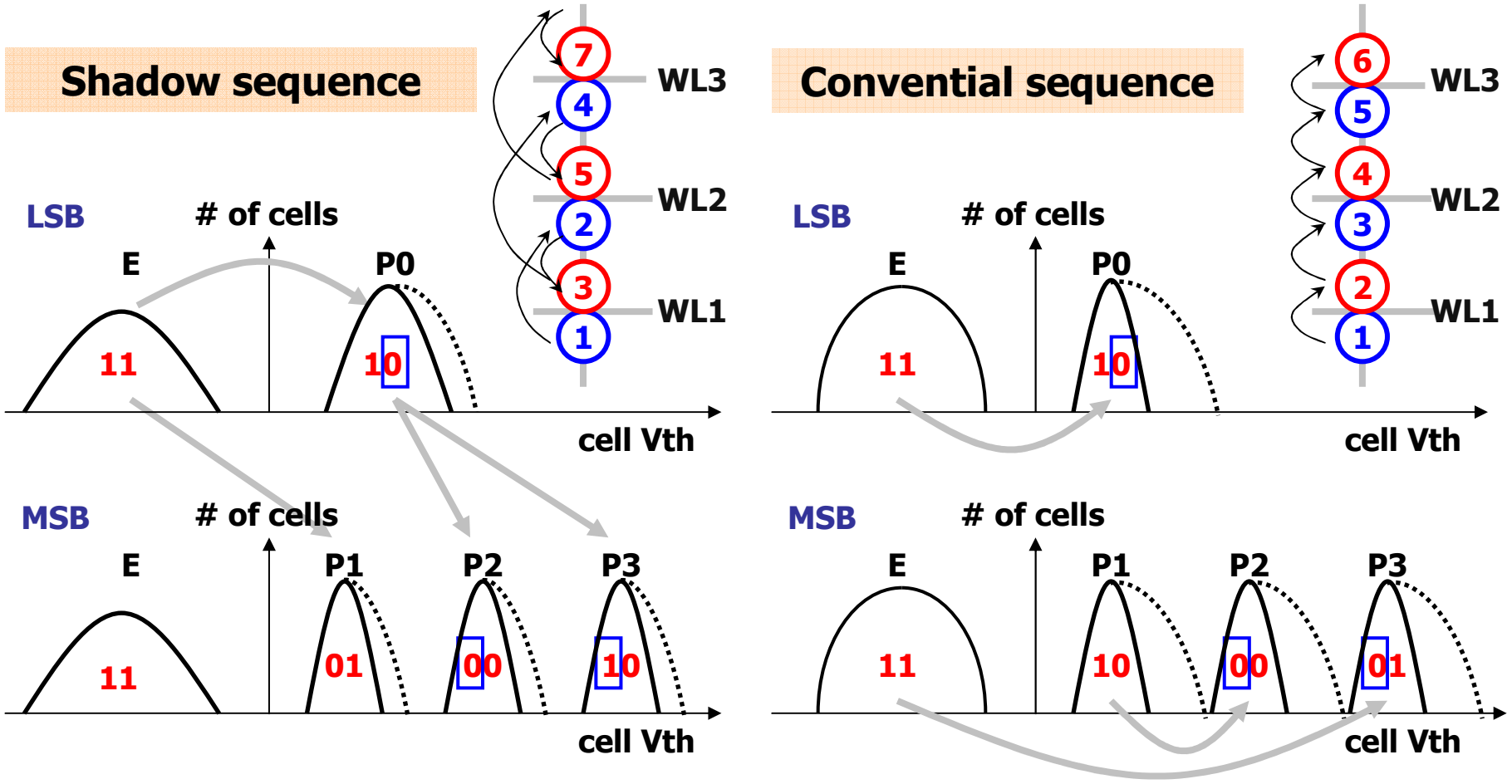
Cell size vs. F-poly coupling

'09 ISSCC



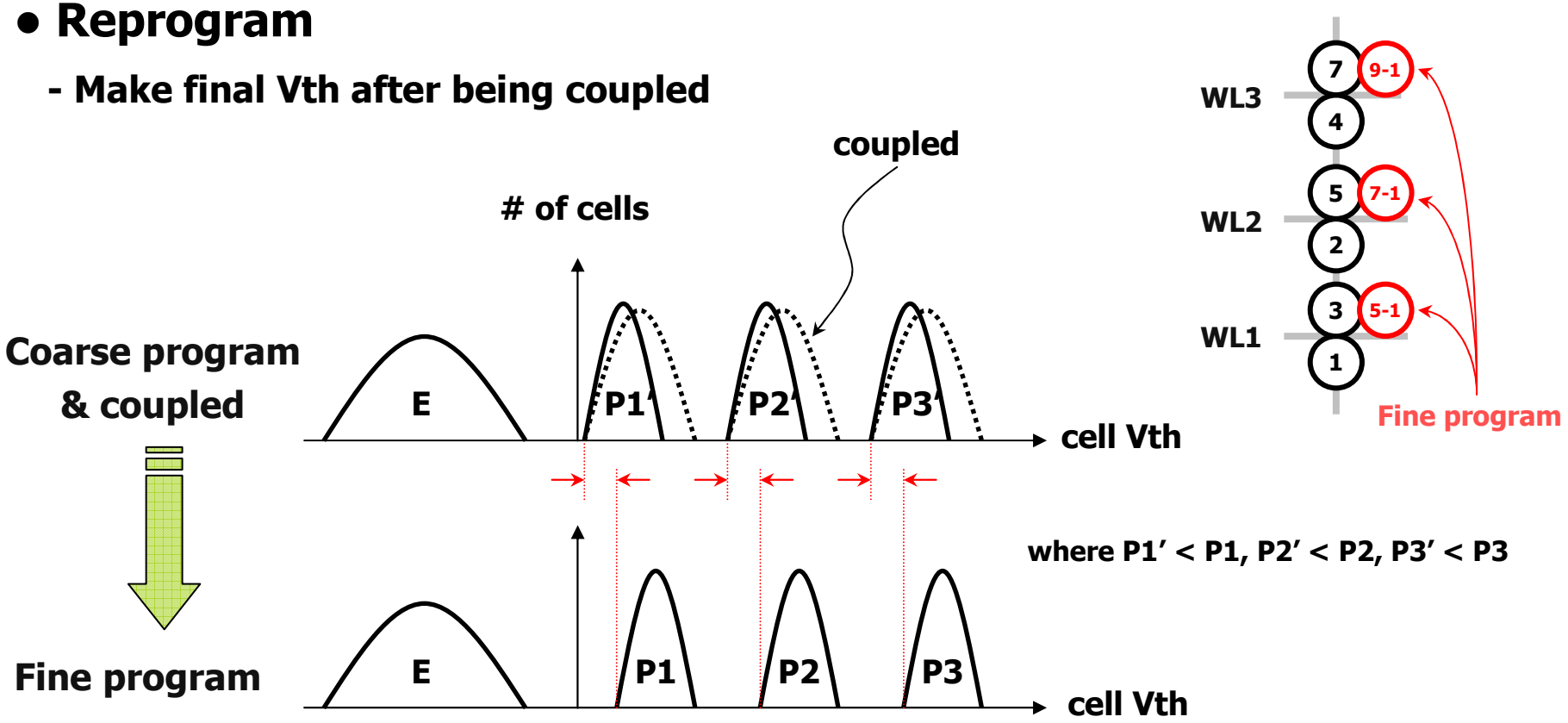
F-poly coupling reduction – (I)

- **Shadow program**
  - Make final Vth after being coupled



F-poly coupling reduction – (II)

- **Reprogram**
  - Make final Vth after being coupled

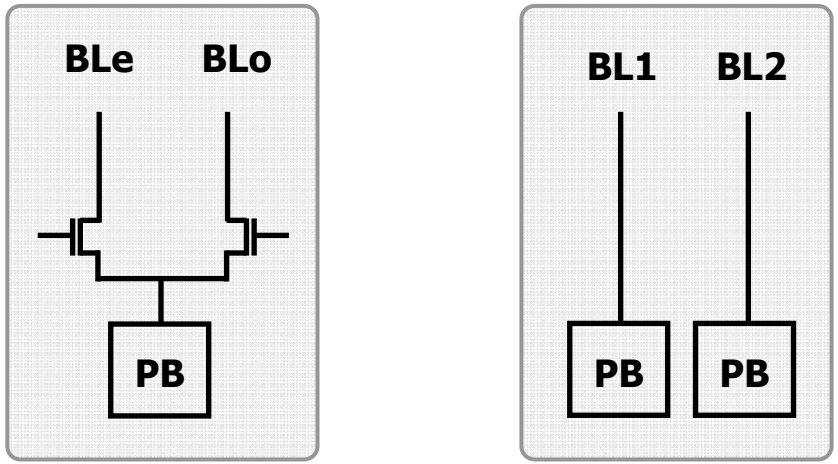


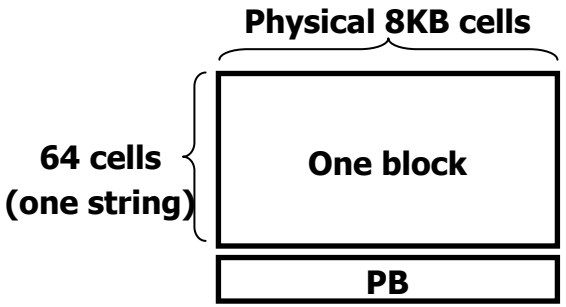
Program performance overhead due to "Fine program"

F-poly coupling reduction – (III)

- **All-bit line (ABL) architecture**
  - all cells in a WL are programmed at the same time
  - in SBL, cells in even BL first, cells in odd BL next (BL-coupling exists)

SBL(Shielded-bit line) **ABL(All-bit line)**





Features : SBL vs. ABL

	SBL	ABL
No. of PBs (page depth)	4KB	8KB
pages/block	256 pages	128 pages

In the near future

3D Flash memory

- **Bit-Cost Scalable(BiCS) technology**

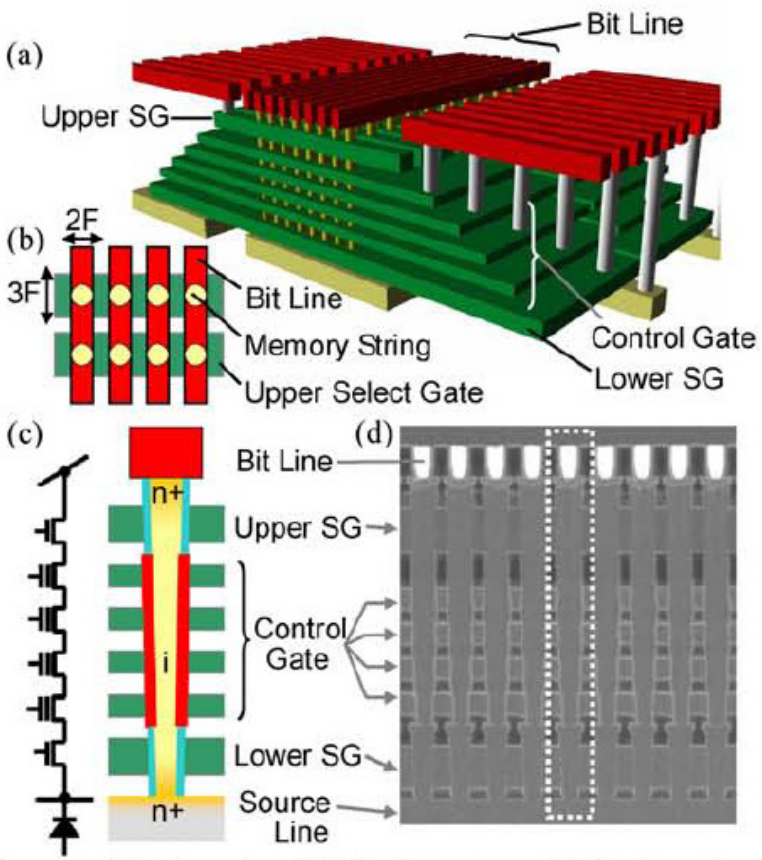


Figure 1: (a) Birds-eye view of BiCS Flash memory. (b) Top-down view of BiCS Flash memory array. (c) Enlarged view of the memory string. (d) Cross sectional SEM image of BiCS Flash memory array.

2007 IEDM, Toshiba

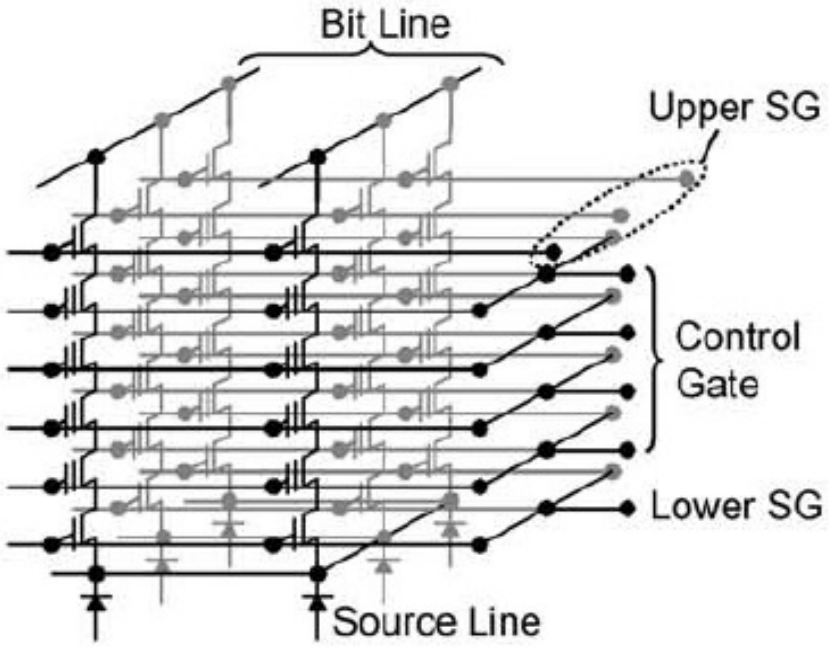
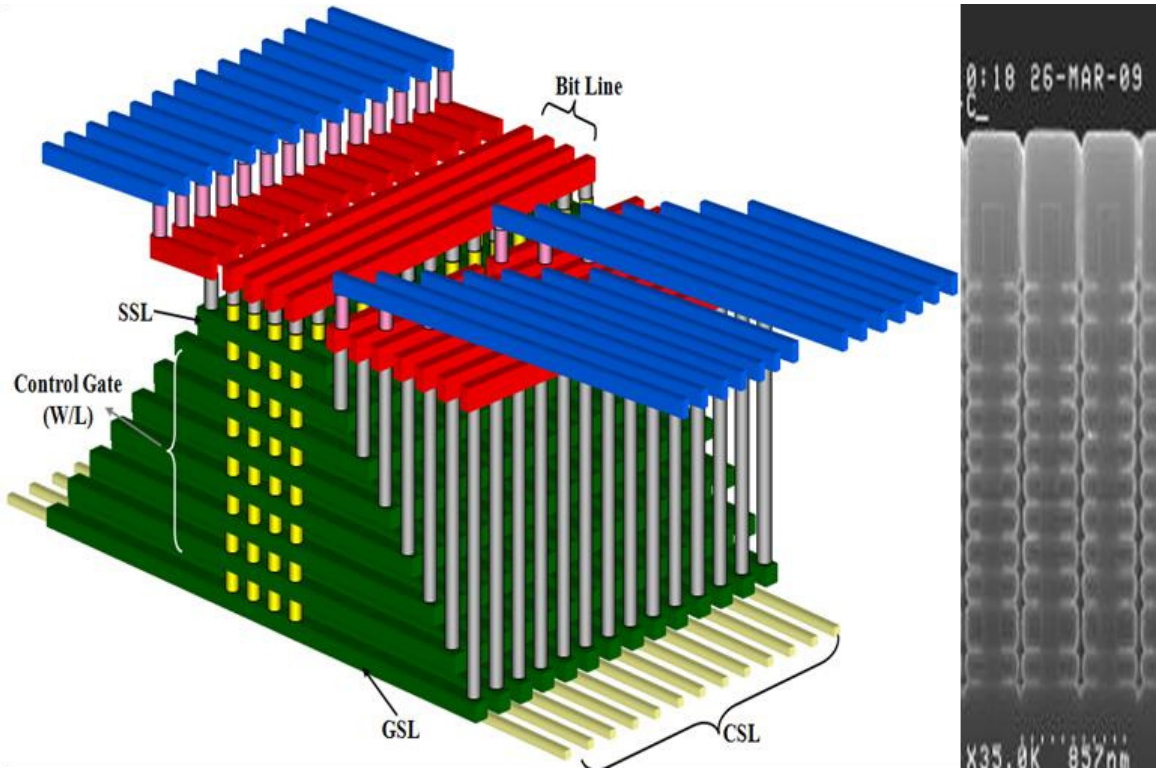


Figure 2: Equivalent circuit of BiCS Flash memory.

3D Flash memory

- **TCAT(Terabit Cell Array Transistor) technology**

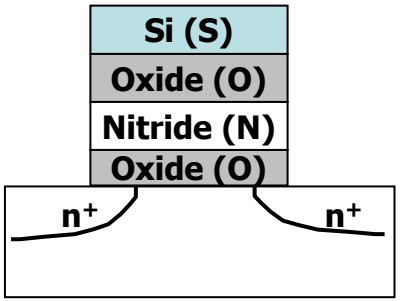
2009 VLSI, Samsung



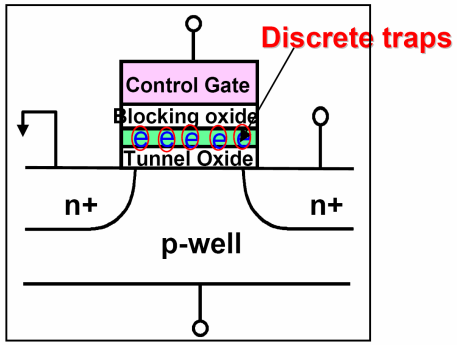
What is CTF ?

- **CTF (Charge Trap Flash)**
  - **SONOS type Flash**
  - **electron is trapped in nitride trap layer**

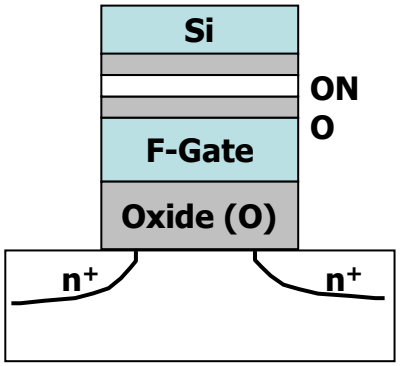
SONOS



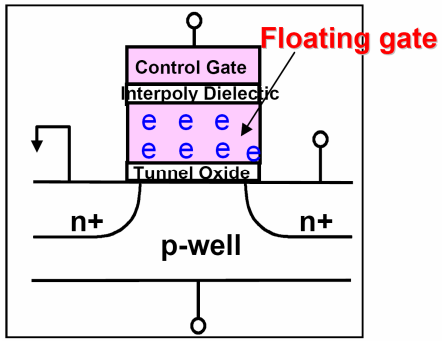
P.C.Y. Chen, TED, V. 24, pp.584-586, 1977



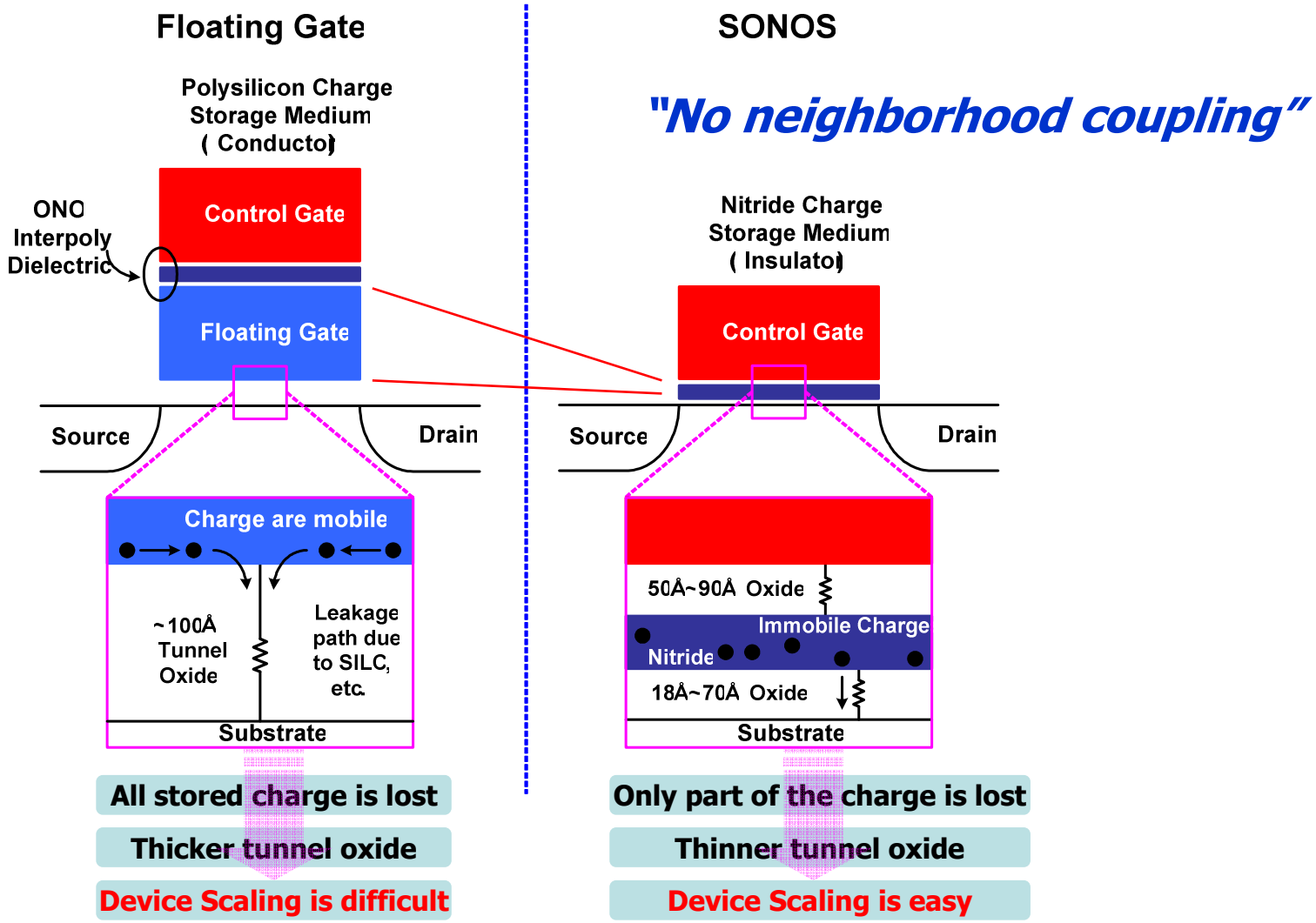
Floating Gate



F.Masuoka (Toshiba)



Floating gate vs. SONOS



Thanks for your listening !