RF and Circuit Integrity in Digital Systems

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Overview

How Digital Circuits & Systems Are Built, and Some Ways in Which They Fail

- **Components of Digital Systems**
- **RF- and Temperature-Related Vulnerabilities**
  - ***Data*** *Inputs and Networks*
  - ***Clock*** *Inputs and Networks*
  - ***Power/Ground*** *Inputs and Networks*
- **Circuit Design: Our Device-Under-Test**

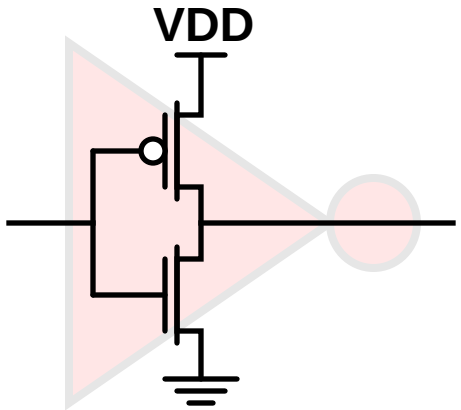
Recent Work

- **Comparison of Vulnerability: DUT's Clock/Data Inputs**
- **[DUT: test chip fabricated in AMI's 0.5µm process]**
- **Custom Chip Design & Fabrication for ESD Studies**

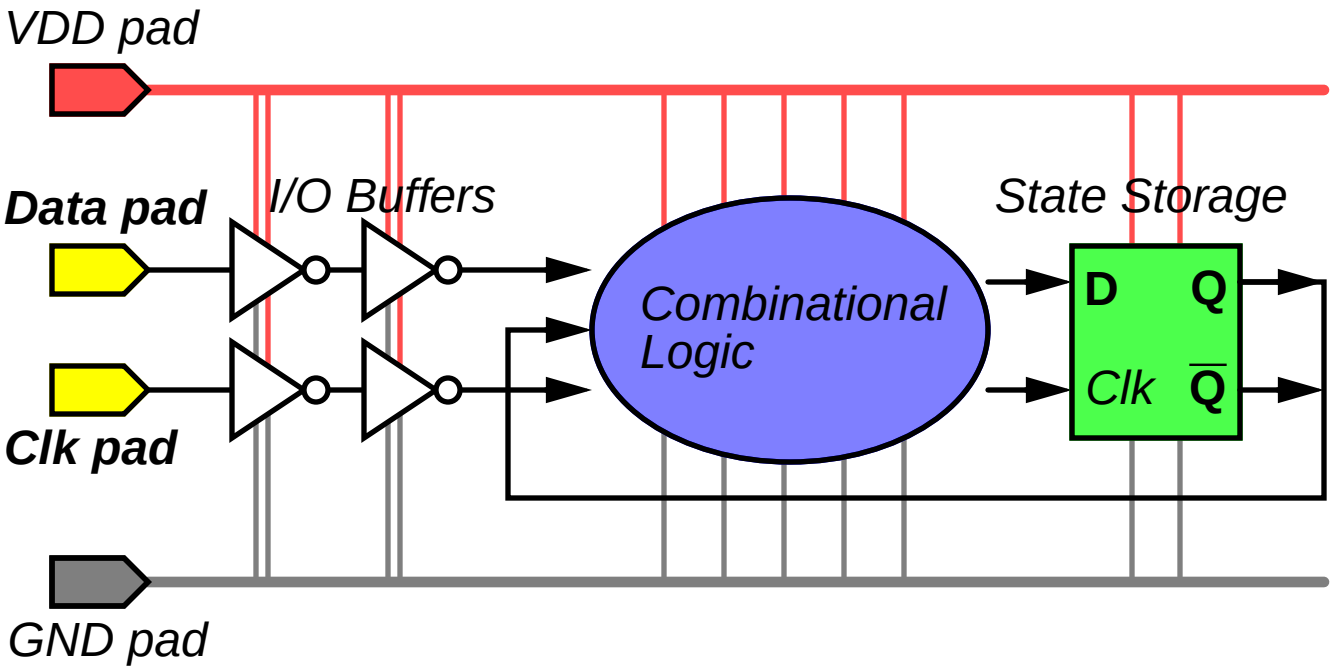
Future Work

Digital Systems: A Primer

Simple Digital *Circuit:*

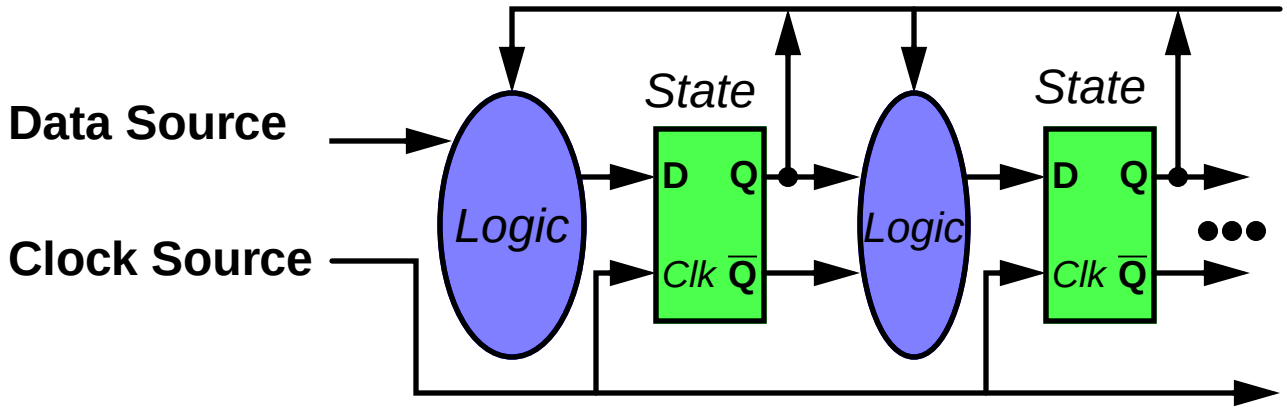


Simple Digital *System:*



Digital Systems: A Primer

Components of Digital Systems

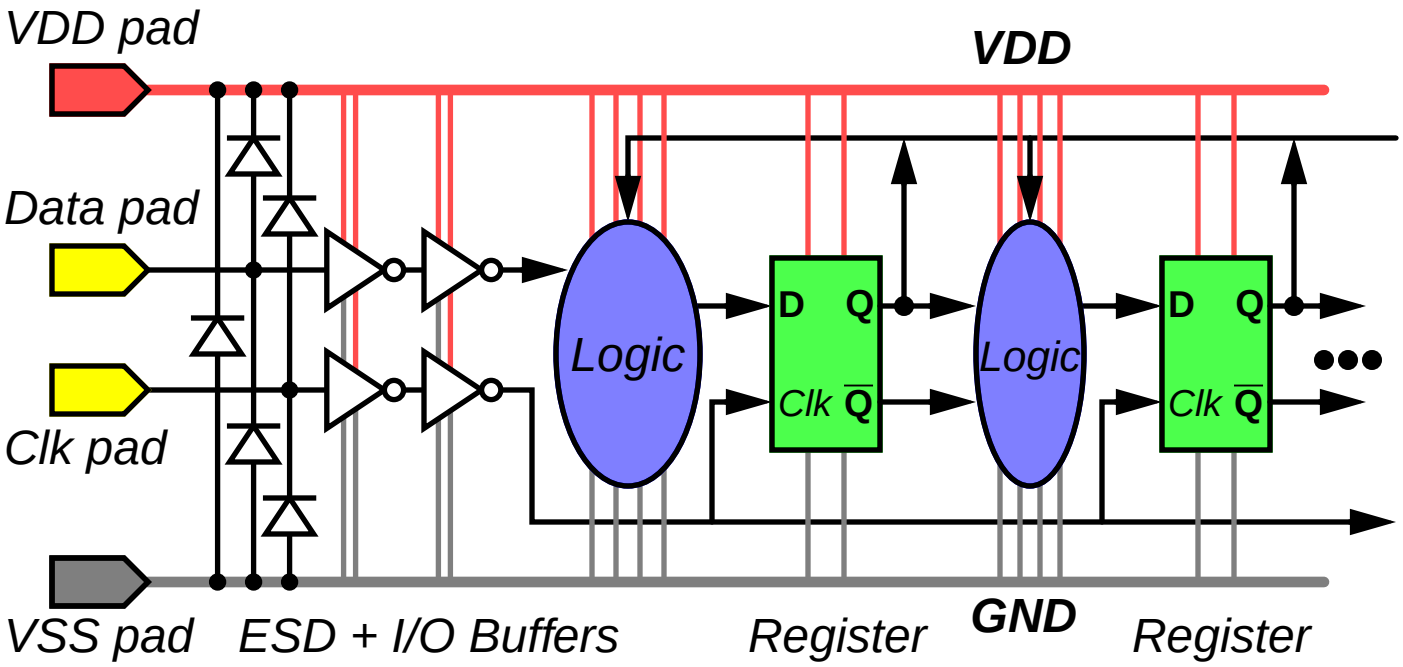


Most systems are *pipelined:*

- **Multiple logic blocks operating simultaneously**
- **Highly synchronous: lock-step operation**

Digital Systems: A Primer

Components of Digital Systems

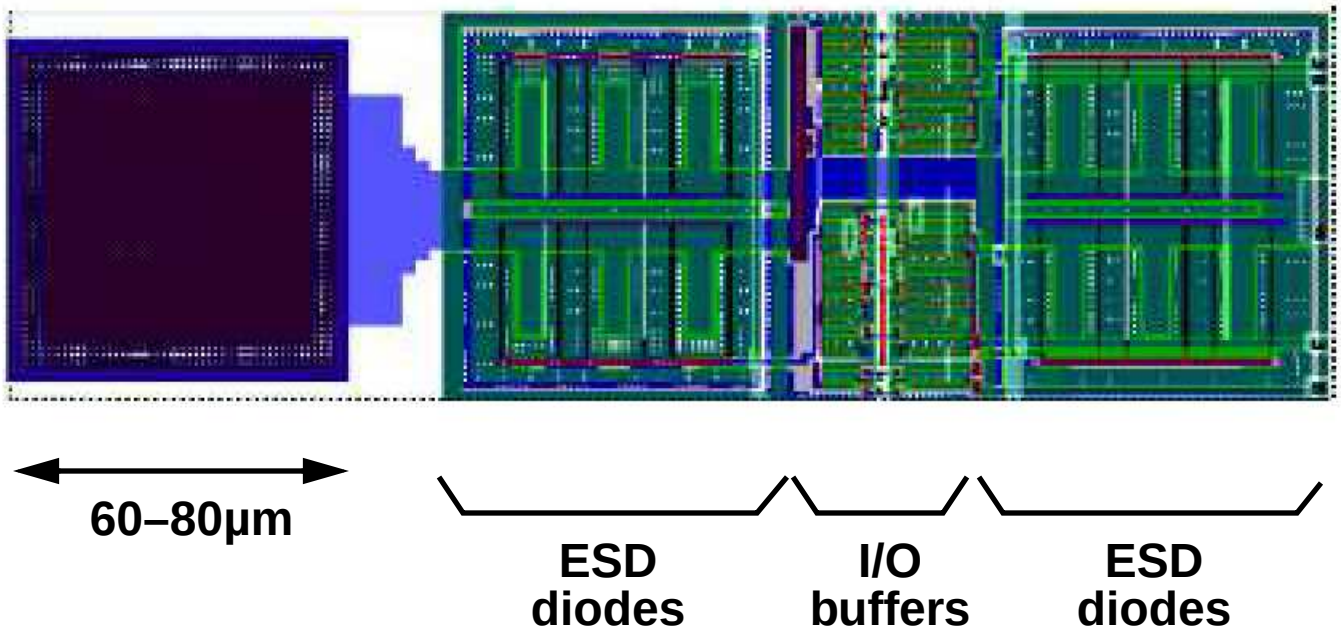


Groundplanes play significant role:

- **Provide references for input amplifiers**
- **Allow CMOS circuits to behave as signal repeaters (with high input impedance, low output impedance)**

Digital Systems: A Primer

Components of Digital Systems

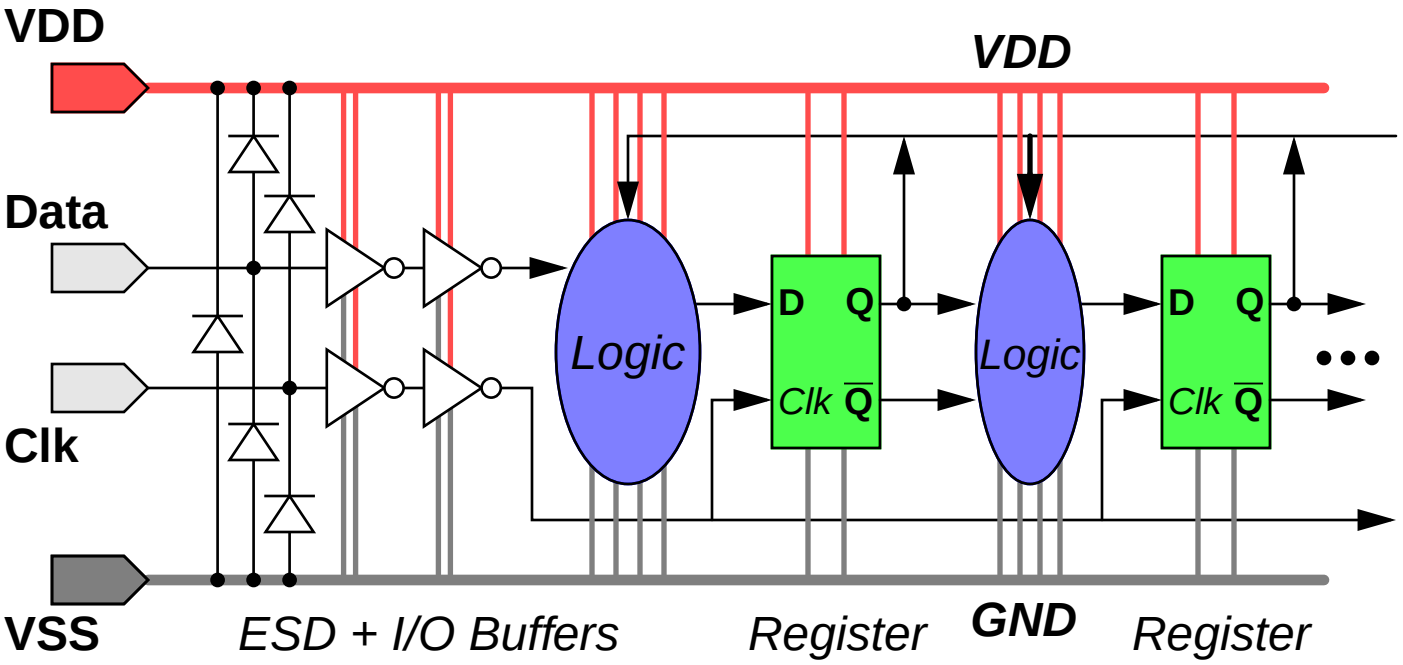


I/O Pads play significant role:

- **Enormous capacitances, require enormous gates to drive them (and the pins & off-chip traces)**
- **Big gates => big currents; fast clocks => small dt … VDD/VSS leads have inductance => Ldi/dt noise**

Digital Systems: A Primer

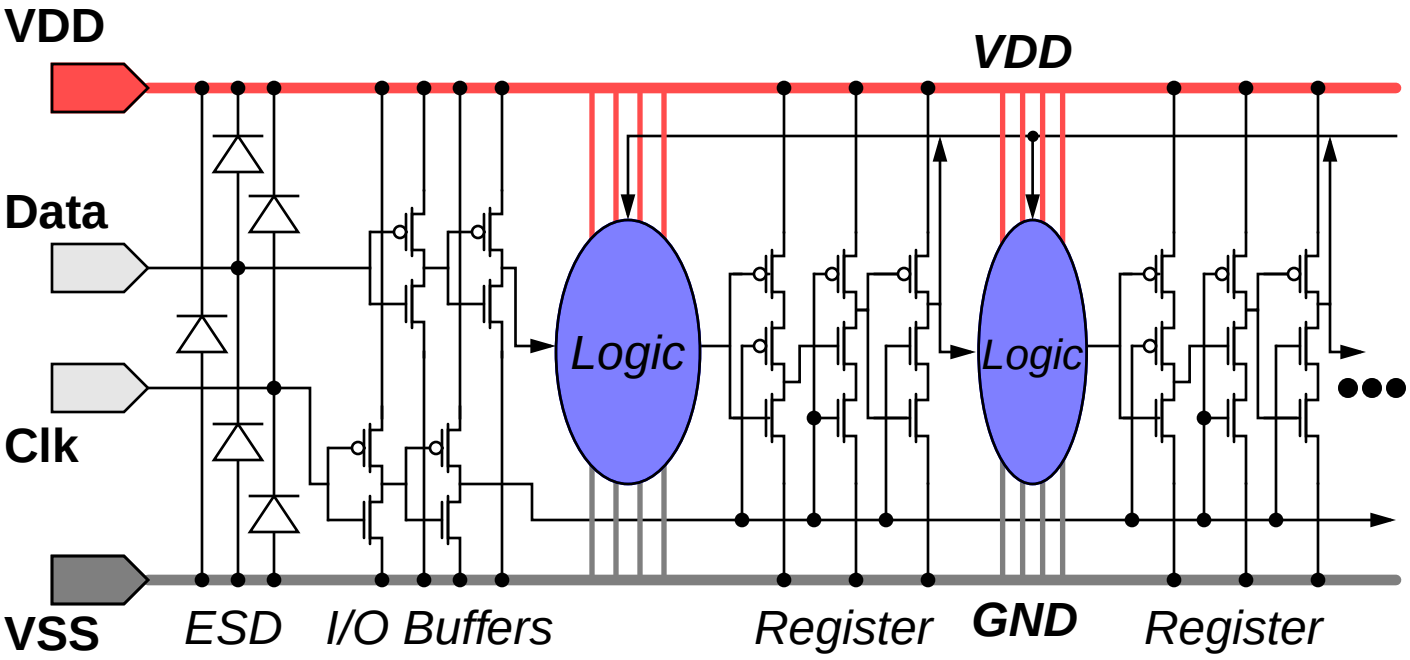
Components of Digital Systems



At the bottom are 'just' a bunch of MOSFETs

Digital Systems: A Primer

Components of Digital Systems

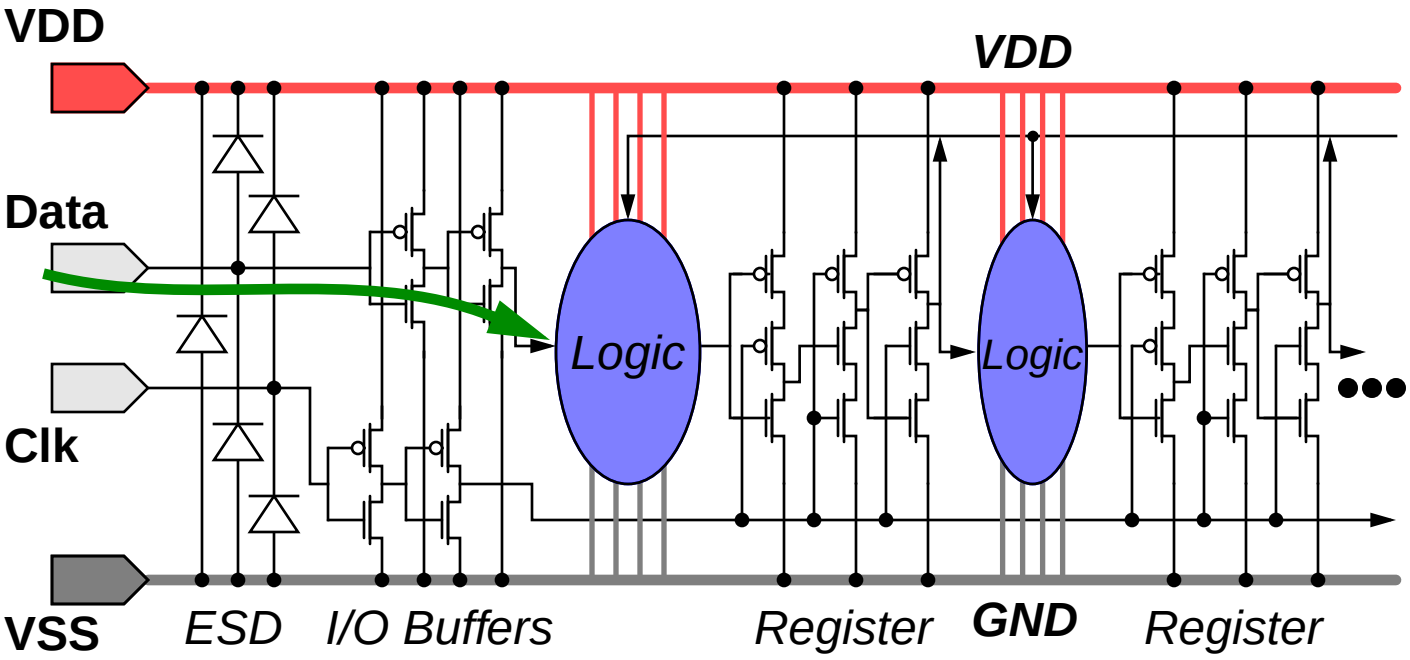


At the bottom are 'just' a bunch of MOSFETs

- Each register shown holds one bit
- Each I/O pad requires its own ESD, receivers, & drivers
- Logic blocks can be arbitrarily large/complex

Circuit Integrity: *Data*

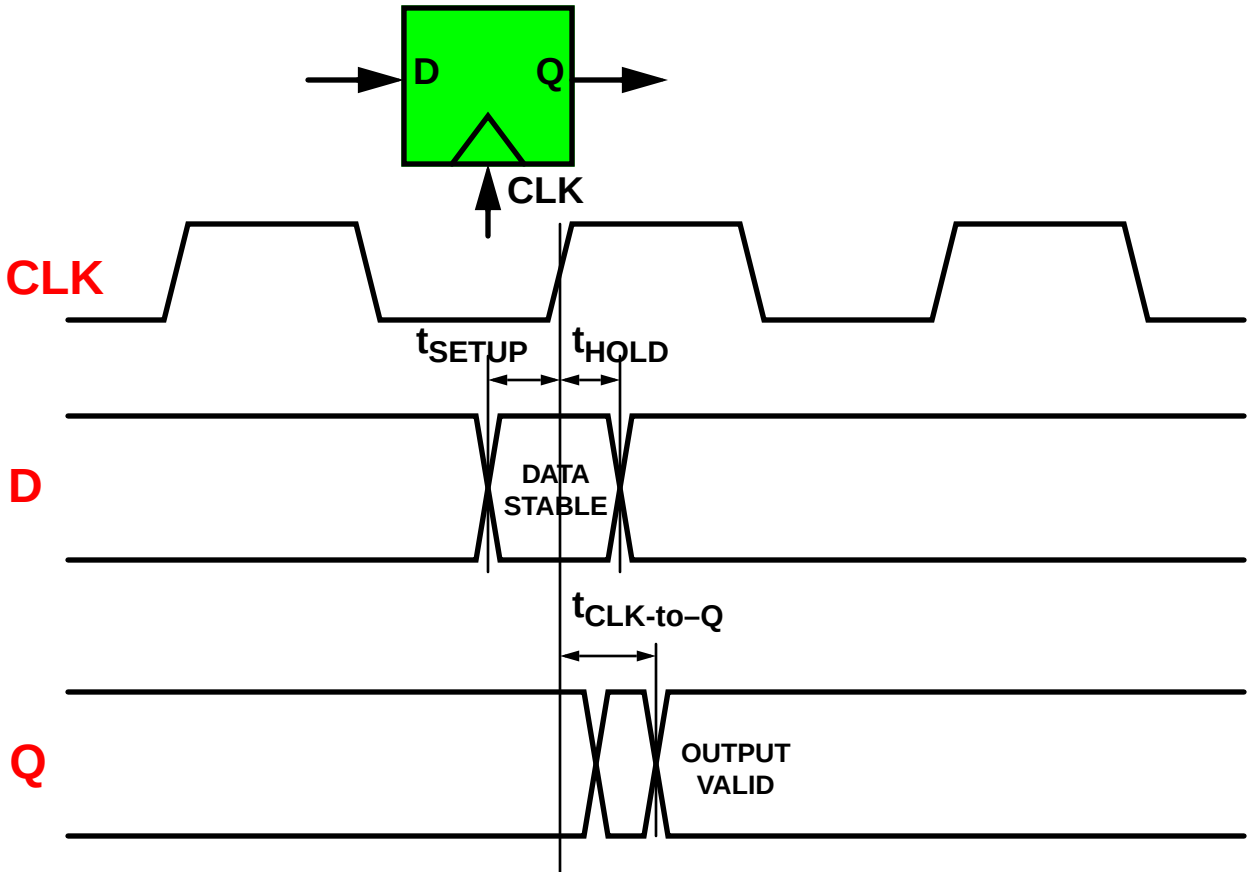
How To Make This System Fail …



- **RF that makes it this far (past initial I/O buffers) has corrupted the system: only solution is to use higher level bus- or packet-encoding techniques**
- **Corrupted data can lead to incorrect results, software crash/reboot, transmission to remote nodes, etc.**

Sequential Circuits Primer

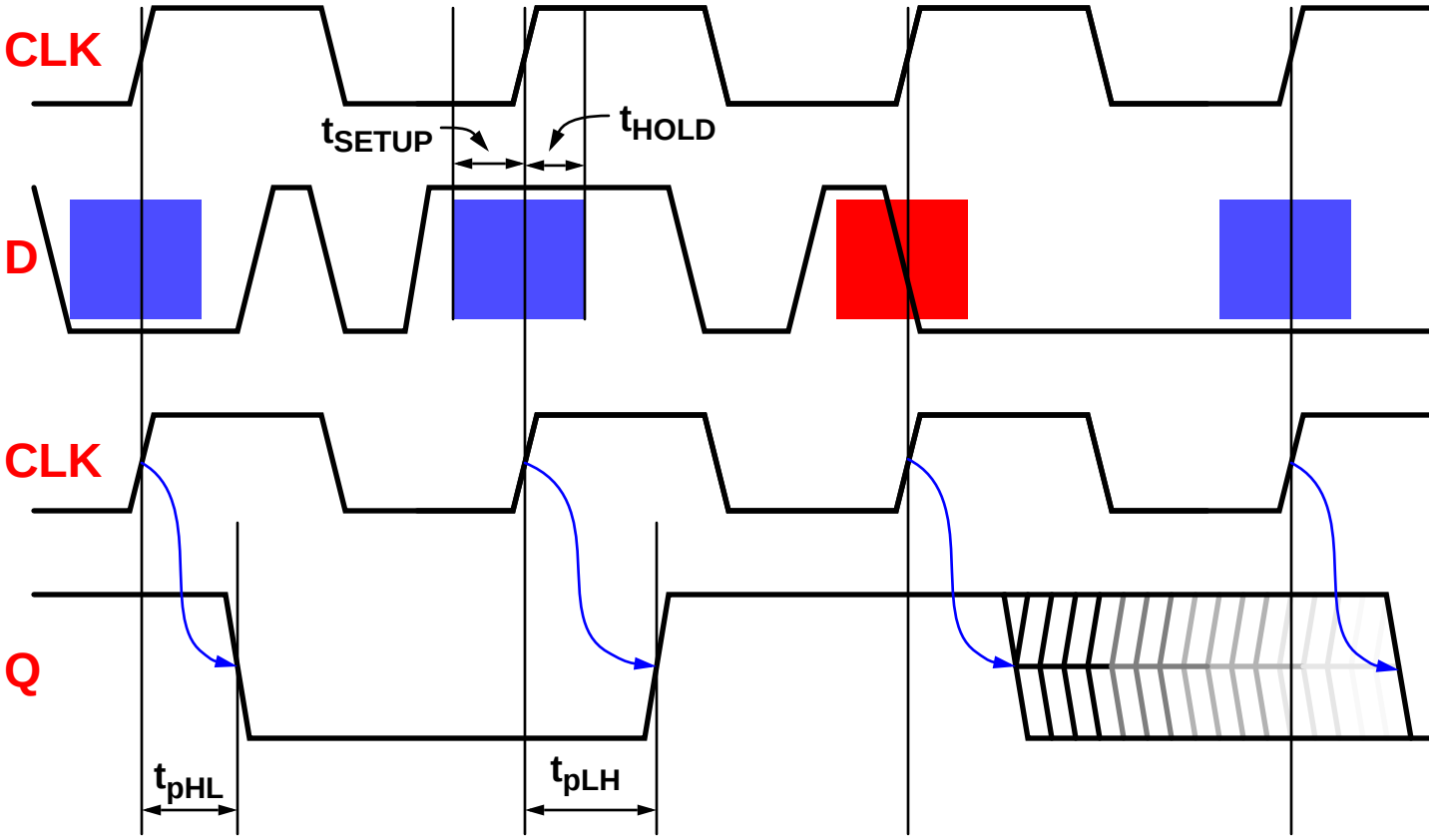
SET-UP and HOLD times



- **Storage elements (latches, registers) expect data and clock edges to be timed perfectly (e.g., within 20ps)**

Sequential Circuits Primer

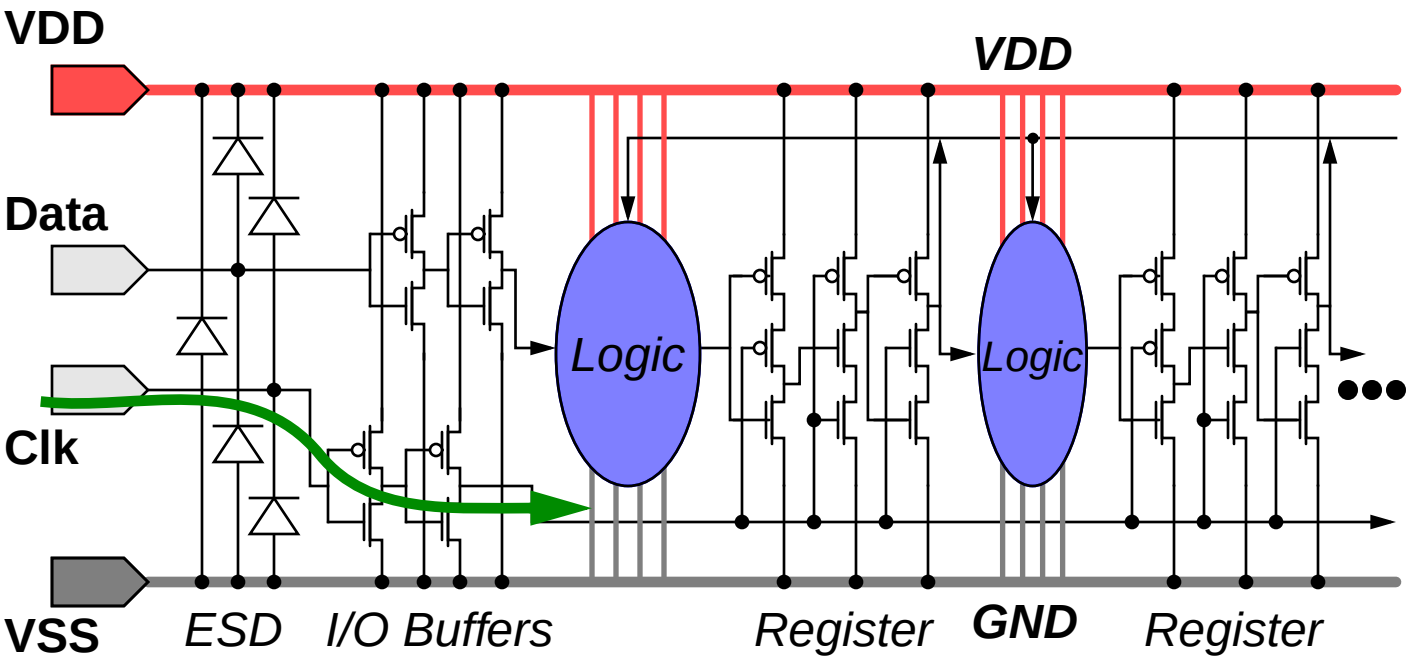
SET-UP and HOLD time, metastability



- **Data must not transition near clock edges**
- ***Corollary:* Perturbations on clock network (e.g., noise spikes, thermal-related delays) achieve same results**

Circuit Integrity: *Clock*

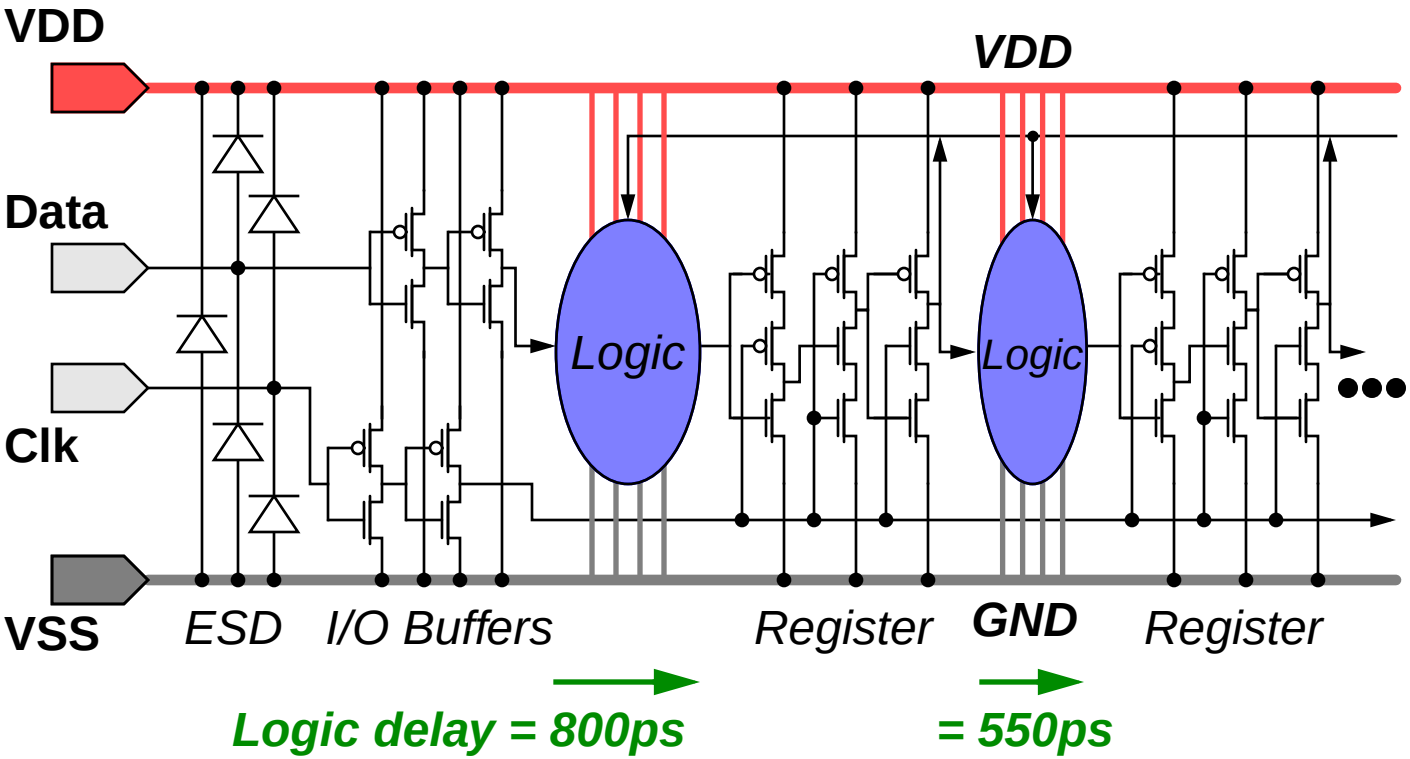
How To Make This System Fail …



- **RF that makes it this far (past initial I/O buffers) has corrupted the system: packet-encoding techniques that might detect data corruption are inapplicable**
- **Unwanted clock edges likely result in metastability, lead to incorrect results, most likely system crash**

Circuit Integrity: *Clock*

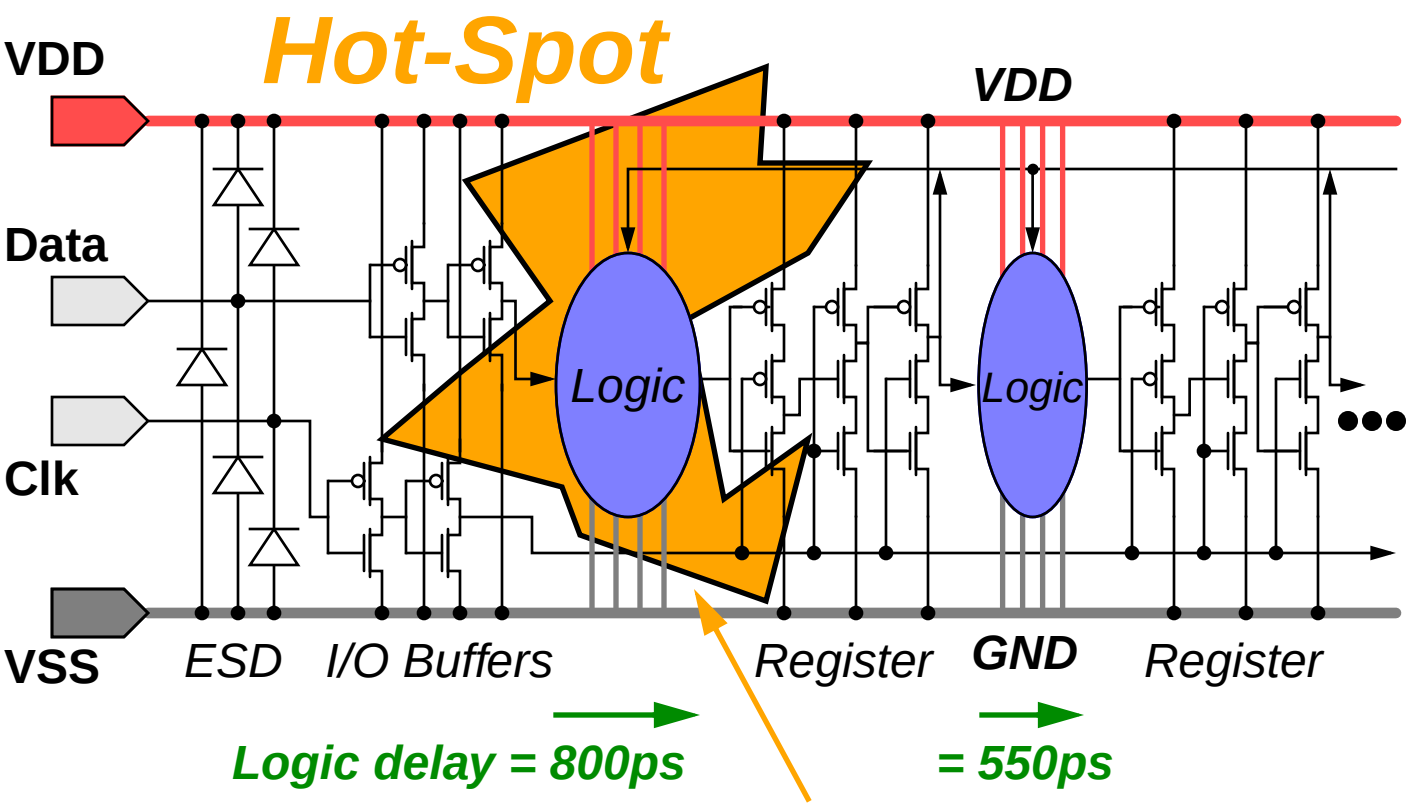
Maximum clock-frequency calculations



- **Critical path determines minimum clock period (in this example: 800ps + register overhead + skew/etc. =1000ps total, or 1GHz [as opposed to 750ps/1.33GHz])**

Circuit Integrity: *Clock*

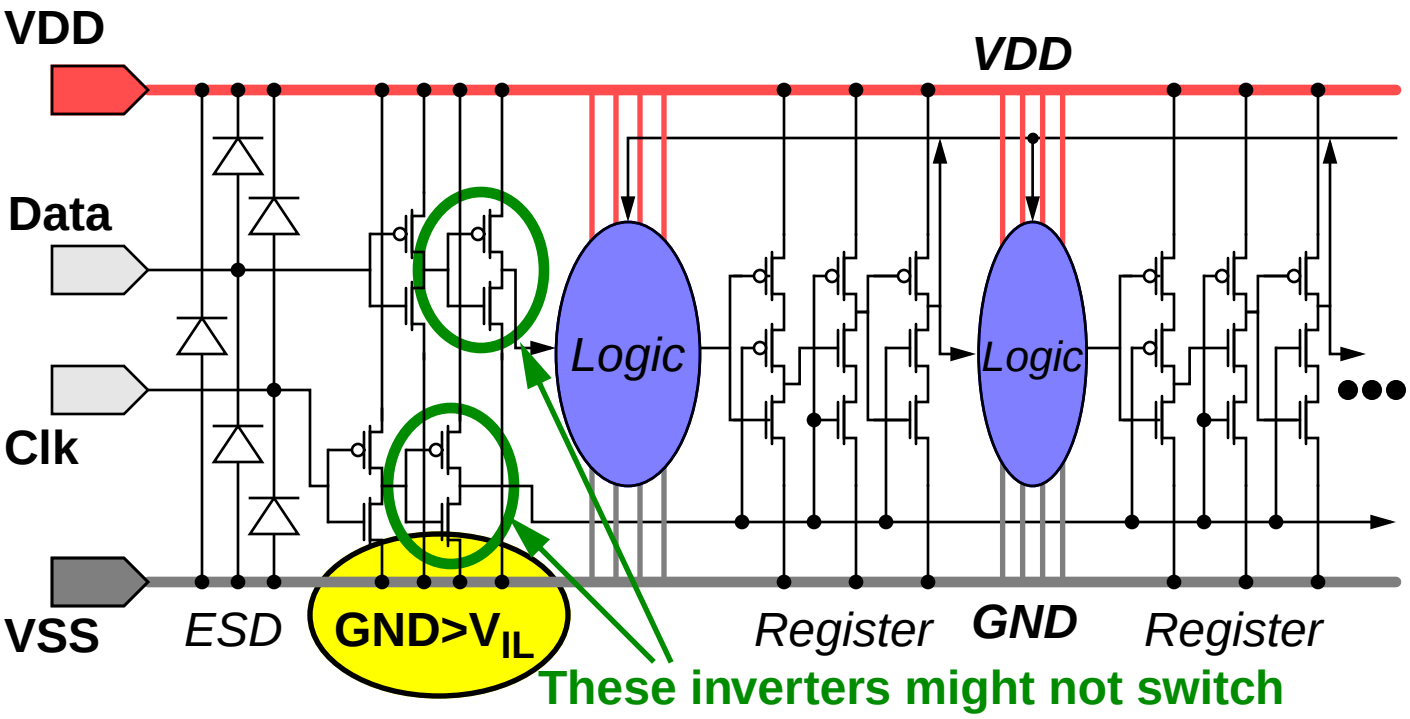
How To Make This System Fail …



- **Thermal gradients in synchronous systems disastrous (consider tight timing margins in GHz systems)**

Circuit Integrity: V_{DD} & V_{SS}

How To Make This System Fail …



- **Localized (or global) ripples on groundplanes can cause logic to misbehave, inputs to be misinterpreted (e.g. suppose Data/Clk = 1, V > V_{IL} on gate of 2nd INV)**
- **Causes same effects as data/clock corruption**

Circuit Integrity

DISTINGUISHING CHARACTERISTICS of the NETWORKS in DIGITAL SYSTEMS:

- **CLK: Only Edges Matter**
- **DATA: Both Timing and Levels Matter**
- **VDD/GND: Even Small Changes in Level (e.g., 5–10%) Matter**

CLK/DATA: Enter Via ESD Protection

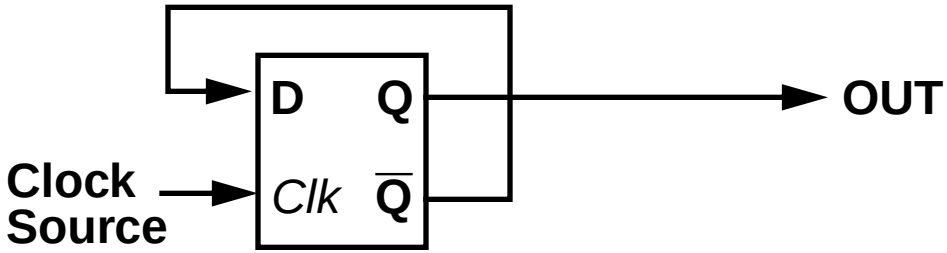
VDD/GND: 1/2 ESD (shunts one to other)

Our Research Question

Comparing CLK and DATA inputs, which is more important:

- **The distinguishing characteristics of the way those inputs will be used in the digital system or circuit?**
- **The levels and frequencies of injected RF?**

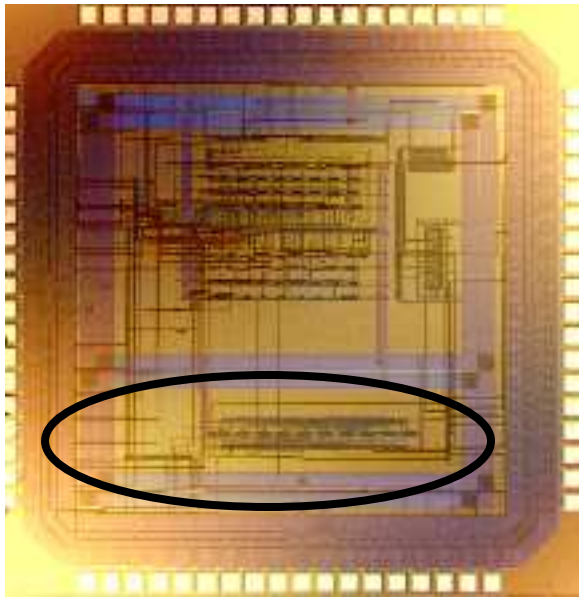
Our Device Under Test (counter):



Just about simplest possible digital system

[*Last Year's Results:* evaluated vulnerability of CLK input]

Our Device Under Test



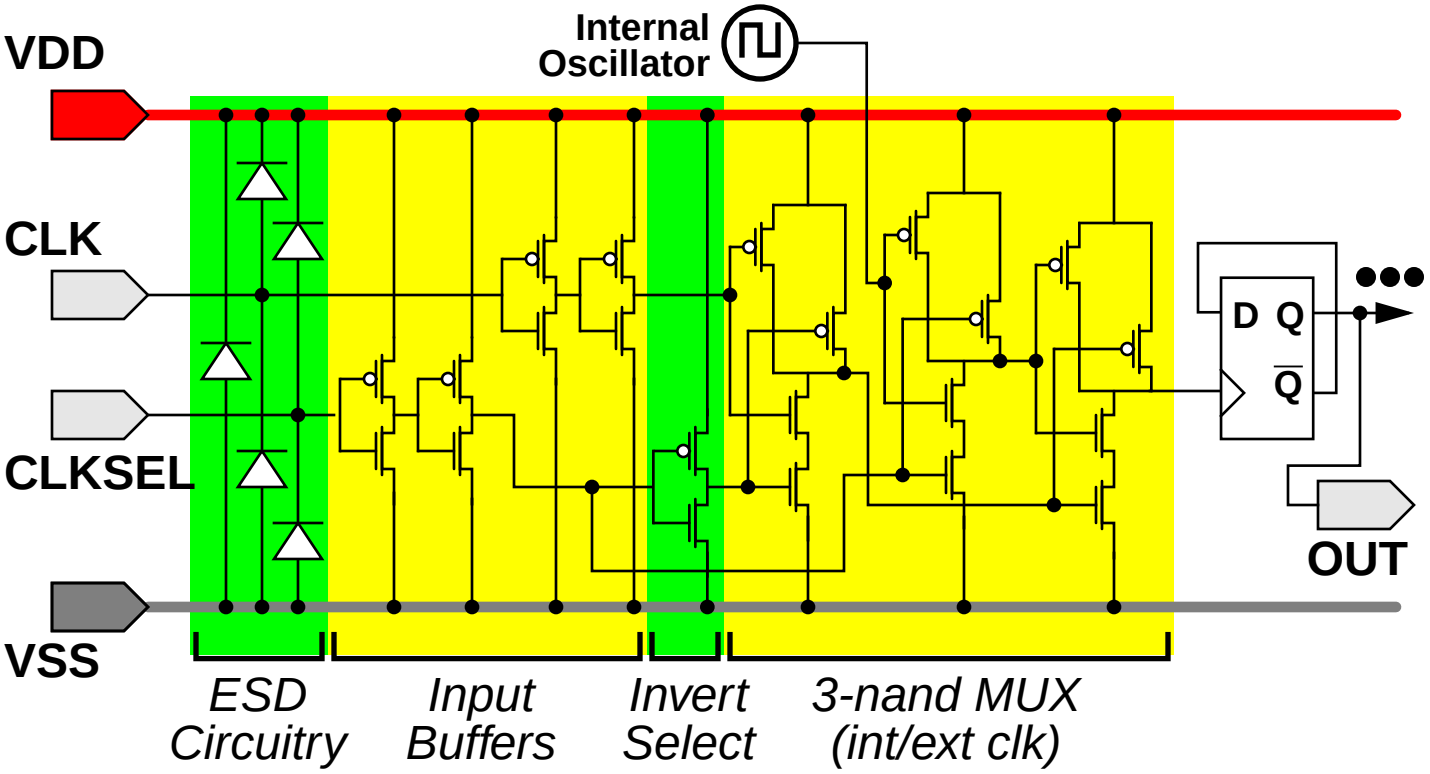
8-bit Ripple Counter, Chip Built via MOSIS

Full-Custom Design (except for pad frame)

Fabricated in AMI's 0.5µm Technology

3.3V power supply

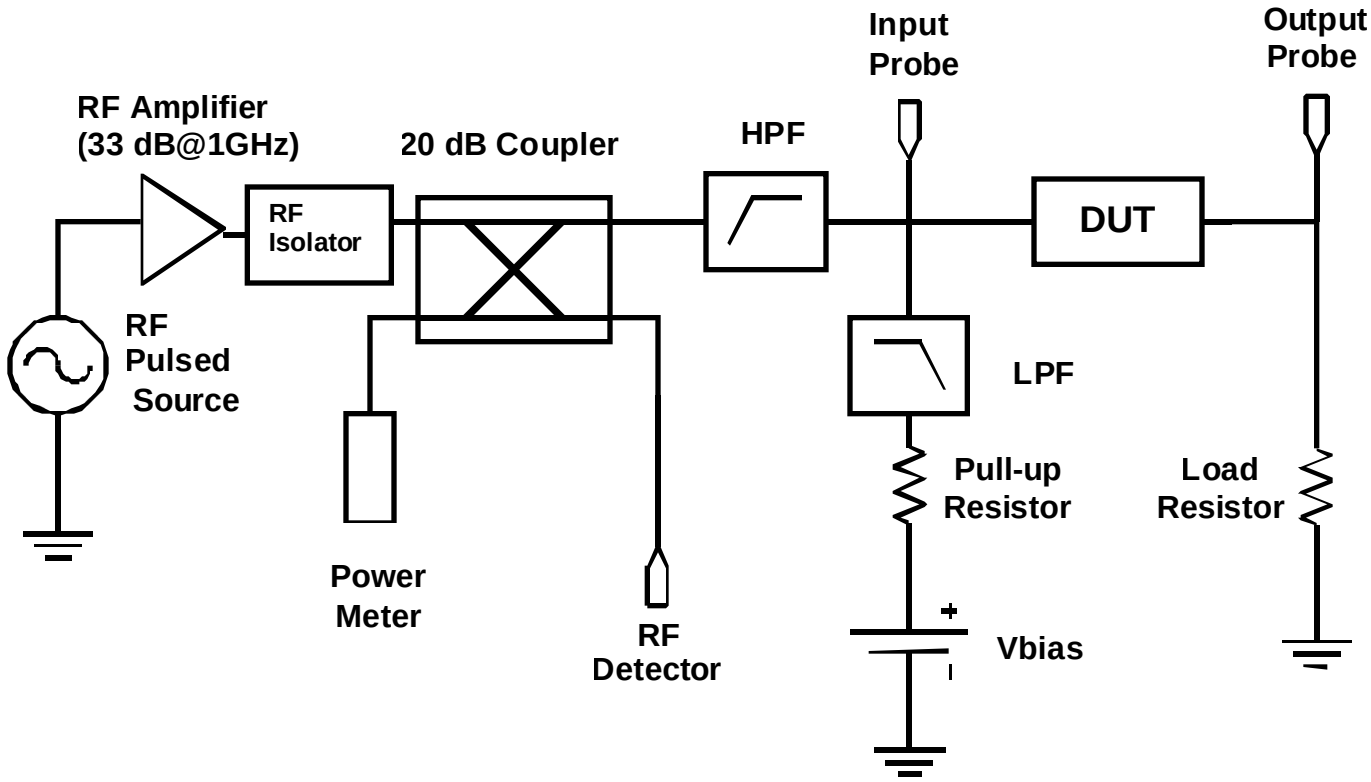
Our Device Under Test



Points of Interest:

- **Digital system built from complementary gate designs (high input impedance, low output impedance).**
- **CLK only driving MUX, one DFF (*see previous slide*).**
- **=> CLK and CLKSEL see virtually identical loads.**

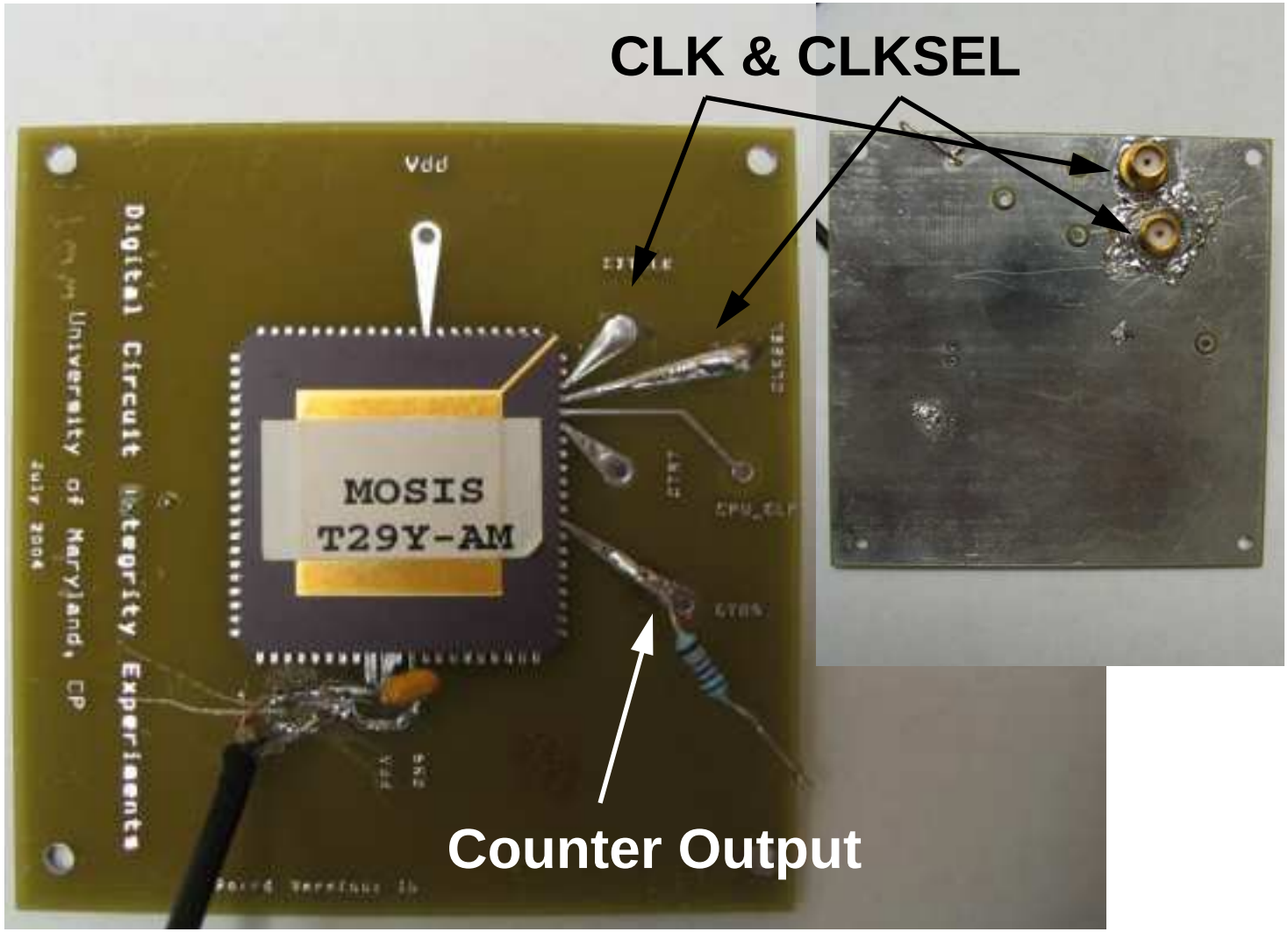
Experimental RF Set-Up



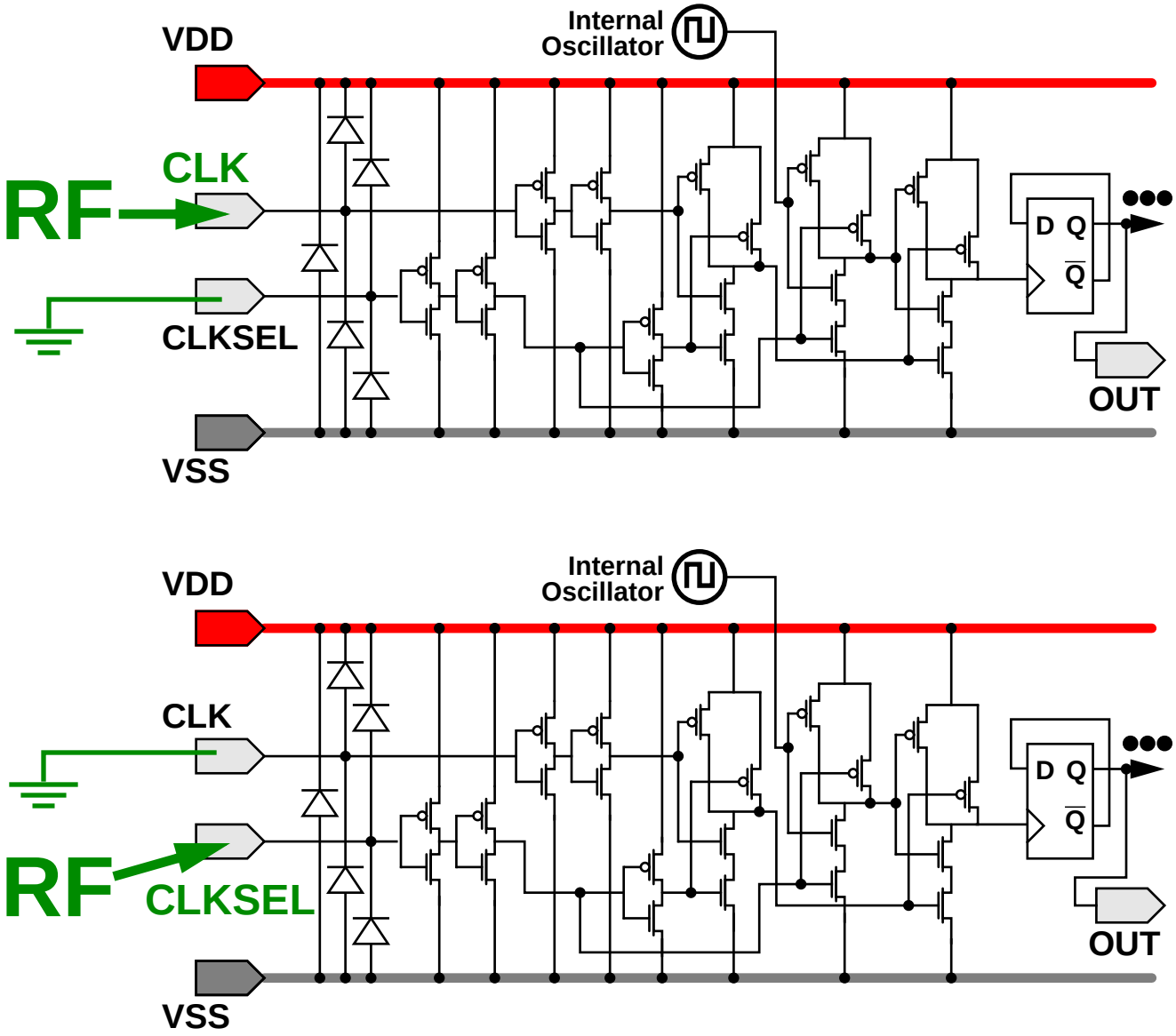
Power Amp 33dB at 1GHz

Freq 800MHz – 4.2Ghz with 1.2W max power

Test Board

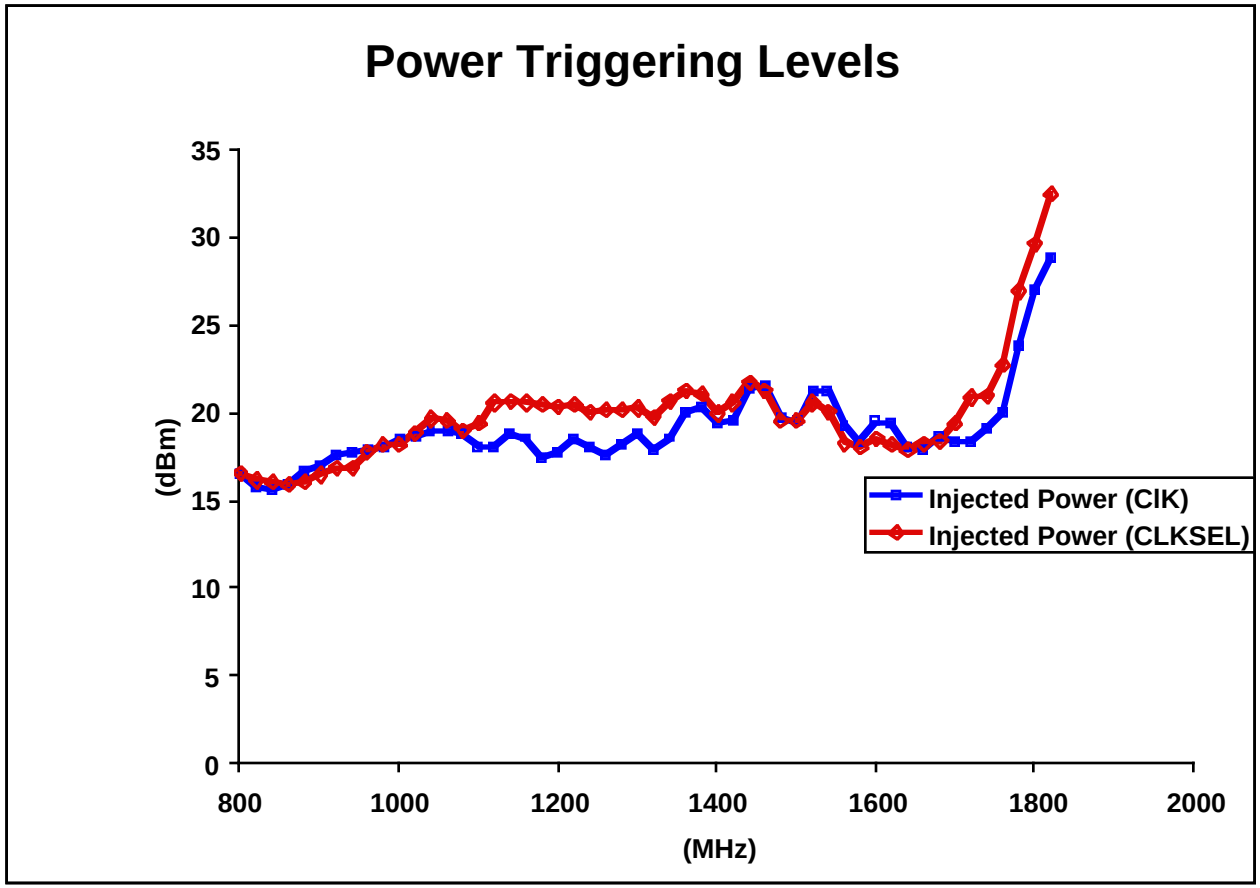

CLK & CLKSEL
Vdd
MOSIS
T29Y-AM
Digital Circuit Integrity Experiments
University of Maryland, CP
July 2004
Counter Output

Test Scenarios



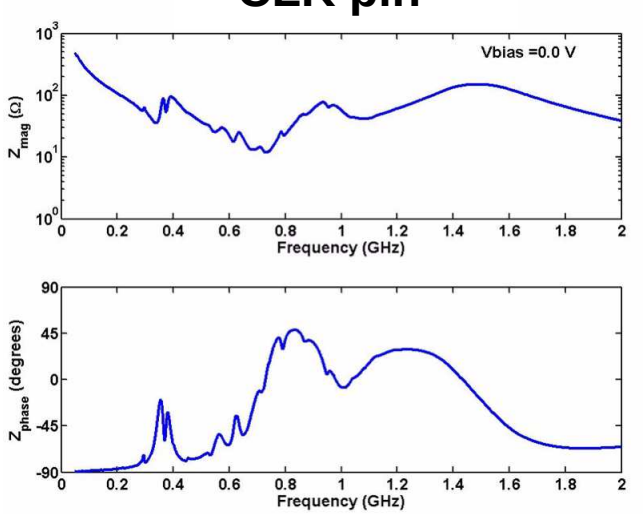
CLK vs. CLKSEL Inputs

Power-v-Freq. required to cause incorrect behavior (state change in digital logic)

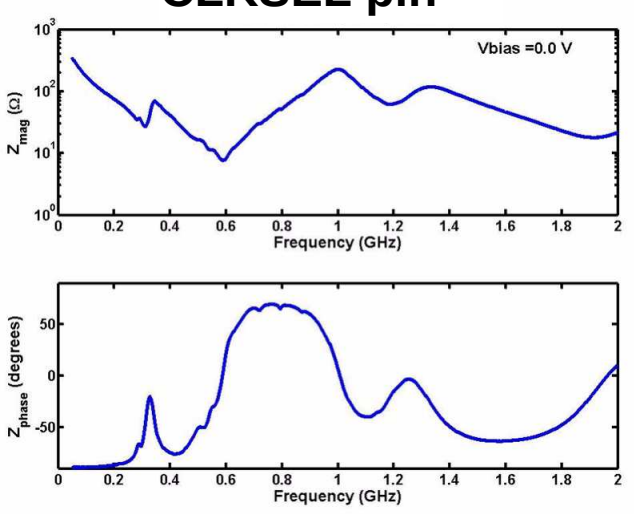


Input Impedance

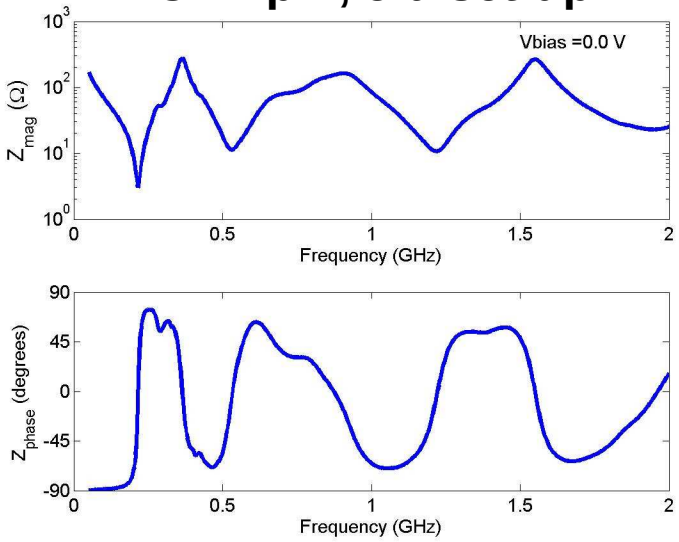
CLK pin

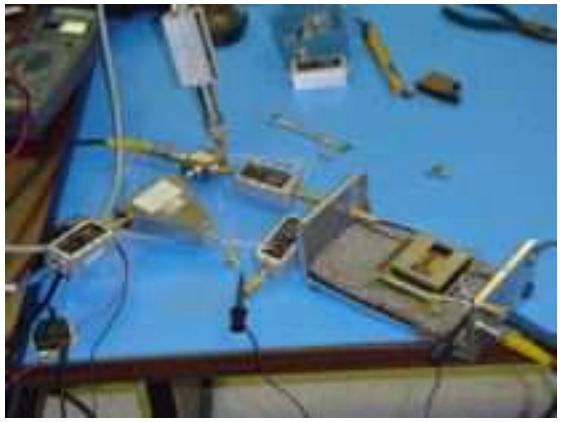


CLKSEL pin



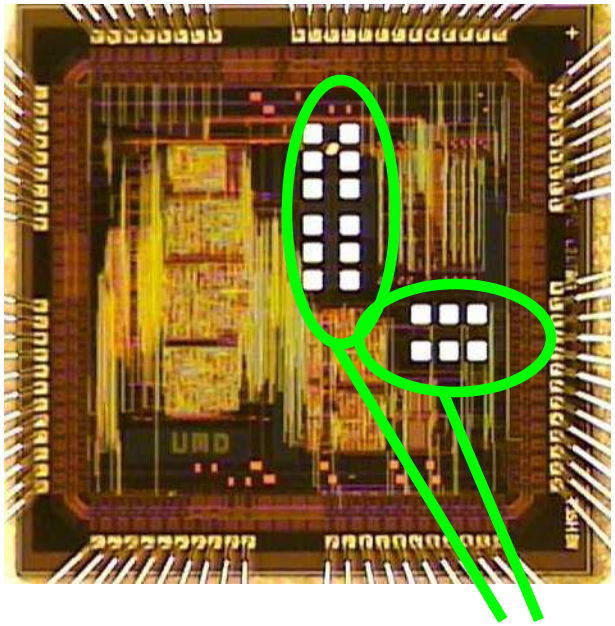
CLK pin, old set-up



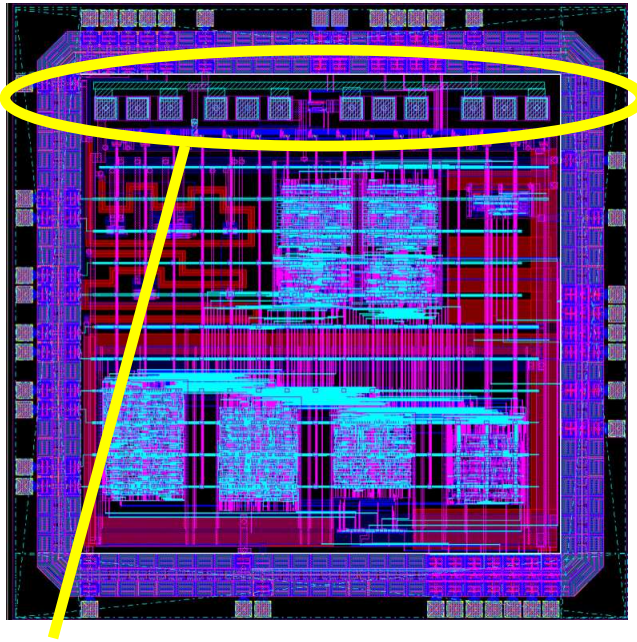


Recent Work: ESD

ESD Test Chip I (die photo) for Rodgers & Firestone



ESD Test Chip II (layout) for Rodgers & Firestone

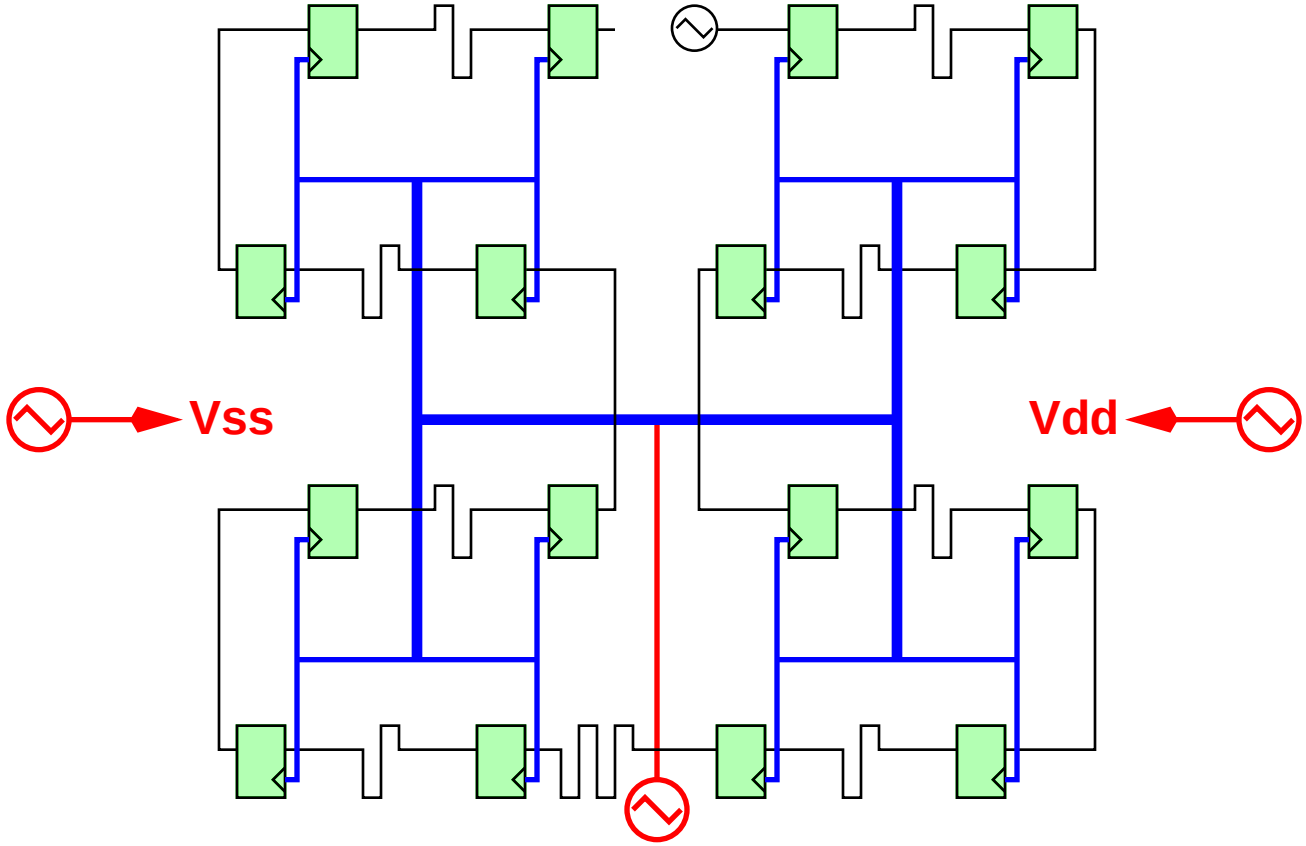


Custom-designed on-chip pads to accommodate input probes

Designed & fabricated two chips (one on right just back from fab) … allow probing at various points between PAD and internals

Future Work

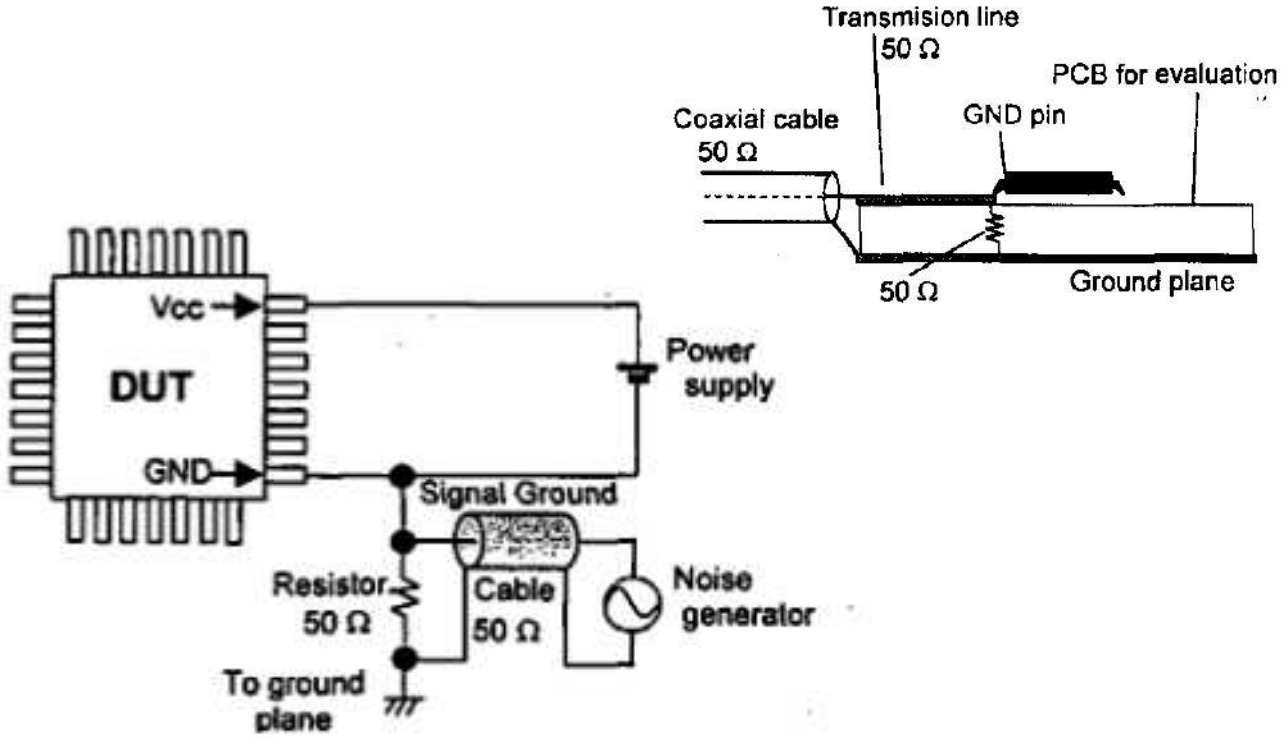
New Test Structures (e.g., to emulate larger designs, differentiate between CLK & DATA)



Future Work

Using same board, test the power rail

Design new board that differentiates GND input pin from IC's ground plane, to test the ground pin's susceptibility



Acknowledgments, etc.

GRAD STUDENTS:

Vincent Chan, Cagdas Dirik, Samuel Rodriguez, Hongxia Wang

INVALUABLE AID:

Todd Firestone and John Rodgers

FOR MORE INFO:

http://www.ece.umd.edu/~blj/integrity

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